PC Curve tracer

Thesis Project Report

Author: Xiaojing Yu 00069460
School: HZ University of Applied Sciences
Company: Company name: NXP Semiconductors Netherlands B.V.
Supervisory Teacher: Bert Verhage
In-company Mentor: John van Zwam, Brecia Nurastu Sasongko
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Implemented by Xiaojing Yu
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Student information
Student name: Xiaojing Yu
Student number: 69460
E-mail: yu0010@hz.nl

School information
Education Institution: HZ University of Applied Sciences
Major: Mechatronics Engineering
Course code: CU08813-Thesis Project
Address: Edisonweg 4, 4382 NW Vlissingen

Internship Information
Project title: PC curve tracer
Supervisory teacher / 1st Examiner: Bert Verhage
Supervisory teacher / 2nd Examiner: D. de Wispelaere
Internship duration: February 2015- July 2015

Company Information
Company name: NXP Semiconductors Netherlands B.V.
In-company mentor: John van Zwam, Brecia Nurastu Sasongko
Address: Gerstweg 2, 6534 AE Nijmegen

Signature:
In-company mentors: Supervisory teacher:

DATE: DATE:
Abstract

In the modern society, the electronics industry is reshaping the way we live. NXP devotes itself to innovate for the benefit of customers, communities and society overall. The research and development is with emphasis on areas that contribute to improving life for all, driving a smarter way of living.

NXP is the undisputed number one supplier and has the extensive portfolio of logic, transistors & diodes and power devices. All major Automotive, Identification, Industrial, Wireless Infrastructure Consumer and Computing manufacturers trust NXP as their major standard products supplier.

Under these circumstances, some customers from those related company usually order a large number of components from NXP. It certainly will have some failing products among many components. Therefore, a test setup – PC curve tracer will be described in this report, which will test DUT efficiently.

The paper is to illustrate the research results of PC curve tracer in DUT test. For the purpose of decreasing the complaint from customers and cut down the analysis expenses, Delft Design Method (DDM) was carried out as the design method. The result showed that under the design of circuit schematic, PCB layout and FPGA programming, the PC curve tracer could source voltage and measure current of each pin of DUT, The failing pin of DUT can be found by testing. To achieve this, AC voltage and DC voltage were generated by the device. Switch is very important to dominate the on-off between pin so that all the voltage between pin and pin can be measured.

The result of the present work implied that the users-based portable measuring and test equipment is being a tendency.

Foreword
In the past 4 months, I did the graduation internship in the automatic vehicle department of NXP Semiconductors B.V. During the period I gained much knowledge about designing a testing set-up, some basic electrical knowledge and the software which produces a PCB board—Altium Designer. I was joyful to apply the past 3 years’ school efforts to practice. Doing this project is a challenging job. Precisely because of the challenging job, I gained more professional knowledge and practical experience, which will have a huge influence on my future career.

The structure of the report shows below will help readers to have a general overview. This report has six chapters:

Chapter 1: Introduction – it gives the basic information and basic analysis about the project.

Chapter 2: Theoretical Framework – it shows the research work did for the project and describes the knowledge will be used in the project.

Chapter 3: Methodology – it introduces and judges the method will be used in the project.

Chapter 4: Results – it shows the design process and displayed the result step by step based on the design method.

Chapter 5: Discussion – it shows the comparison between the results and the requirements.

Chapter 6: Conclusions and Recommendations – it concerns conclusions for the results and gives advice to take or not to take action in the future.

During the internship in NXP, I received much help from my colleagues and mentors. Thanks for the help from Mr. John van Zwam and Ms. Brecia Nurastu Sasongko, they guided me to a right way of the project and gave many helpful suggestions at the technical level. Also thanks for my supervisor – Mr. Bert Verhage, he was conscientious and responsible to help me write a qualified report.

Name: Xiaojing Yu
Date: June 11st, 2105

LIST OF ABBREVIATIONS

ESD: Electrostatic discharge
NTF: No Trouble Found
MOS: Metal Oxide Semiconductor
PC: Personal Computer
DUT: Device under Test
LIN: Local Interconnect Network
CAN: Controller Area Network
USB: Universal Serial Bus
PCB: Printed Circuit Board
FPGA: Field Programmable Gate Array
ADC: Analog-to-Digital Converter
DAC: Digital-to-Analog Converter
EDS: Engineering Design Specifications
DDM: Delft Design Method
SMU: Source Measurement Units
SPI: Serial Peripheral Interface

Contents:

1. Introduction ................................................................................................................. 1
   1.1 Background .............................................................................................................. 1
       1.1.1 Company background ...................................................................................... 1
       1.1.2 Assignment background .................................................................................. 2
   1.2 Research goal ......................................................................................................... 4
   1.3 Research Questions ............................................................................................... 4
       1.3.1 Main question .................................................................................................. 4
       1.3.2 Sub questions ................................................................................................ 5

2. Theoretical framework ............................................................................................. 6
List of figures and tables

Figure 1: TJA 1020
....................................................................................................................... 2
Figure 2: ESD protection (Vishay Siliconix, 2008) ................................................................. 3
Figure 3: The relationship among concepts ............................................................................ 7
Figure 4: The V/I curve on oscilloscope .............................................................................. 7
Figure 5: The curve tracing of diode ..................................................................................... 8
Figure 6: The testing DUT ..................................................................................................... 8
Figure 7: Pinning diagram of TJA1020 .............................................................................. 9
Figure 8: Block diagram of TJA1020 (Philips, 2004) ............................................................ 9
Figure 9: TXD pin ................................................................................................................ 9
Figure 10: ESD-HMM test setup .......................................................................................... 10
Figure 11: ESD-MM test setup .................................................................................................. 10
Figure 12: The MOSFET and its parasitic capacitances (Caka, 2007) .................................. 11
Figure 13: Digital control system with analog I/O (Kuphaldt, 2014) ....................................... 12
Figure 14: Model of the Product Innovation Process .................................................................... 14
Figure 15: Function tree ........................................................................................................ 18
Figure 16: Concept 1 design diagram ........................................................................................ 19
Figure 17: Concept 2 design diagram .......................................................................................... 20
Figure 18: Alitum Designer Development Board NB3000AL.02 .............................................. 22
Figure 19: The design diagram of the best concept .................................................................. 22
Figure 20: Through Hole Mounting resistors (Resistors SMD Leadform Option, 2014) ......... 23
Figure 21: Surface Mounting resistors on PCB ....................................................................... 23
Figure 22: The simplified Schematic circuit design based one NE555 ................................. 24
Figure 23: Internal structure of NE555 .................................................................................. 24
Figure 24: The simulation result of the generator ...................................................................... 25
Figure 25: The schematic of static model .................................................................................. 25
Figure 26: The schematic of switch .......................................................................................... 26
Figure 27: The pin description and function table of TSSA63157 (Texas Instruments, 2005) . 26
Figure 28: The charging process of a RC circuit ...................................................................... 28
Figure 29: Part of SMU schematic ............................................................................................ 28
Figure 30: The simulation of the SMU circuit .......................................................................... 29
Figure 31: The simulation of static model ................................................................................ 29
Figure 32: Absolute maximum ratings of AD8227 ................................................................. 30
Figure 33: Pin configuration of AD8227 .................................................................................. 30
Figure 34: The response circuit from the DUT ........................................................................ 31
Figure 35: The schematic of current limit circuit ................................................................. 32
Figure 36: The simulation of the current limit ................................................................. 32
Figure 37: The schematic of MUX circuit ......................................................................... 33
Figure 38: ADG5208 Truth table (Analog device, 2014) ................................................. 33
Figure 39: ADG5208 Pin Function Descriptions ............................................................ 33
Figure 40: Headers between PC and the device .............................................................. 34
Figure 41: Headers between DUT and the device ........................................................... 34
Figure 42: The details in the dac084s085.SchDoc* ......................................................... 36
Figure 43: Terminal of FPGA ......................................................................................... 37
Figure 44: The project file of FPGA ............................................................................... 37

Table 1: Delft design method ......................................................................................... 14
Table 2: EDS ................................................................................................................. 17
Appendices

Appendix 1: .................................................................................................................. 44
Appendix 2: Morphological Chart ................................................................. 48
Appendix 3: EDS weighing table ............................................................................. 49
Appendix 4: The operational function of NE555 ............................................. 49
Appendix 5: Schematic ......................................................................................... 50
Appendix 6: PCB layout ......................................................................................... 54
Appendix 7: Bills of materials ............................................................................. 55
Appendix 8: CAMtastic1 and CAMtastic2 ....................................................... 58
Appendix 9: The configuration of FPGA and DAC ......................................... 60
Appendix 10: dac084s085.PrjEmb ................................................................. 62
Appendix 11: View page of FPGA ....................................................................... 65
1. Introduction

In this chapter, chapter 1.1 would describe some background information of company and assignment; section 1.2 would list the research goal of this project; according to the assignment background and research goal, section 1.3 would build research questions.

1.1 Background

In this section, the company background and the assignment background would be described. They are the basement of the project.

1.1.1 Company background

NXP Semiconductors is a semiconductor manufacturer, also one of the worldwide top 20 semiconductor sales leaders. It is founded in 1953. The primitive name is Philips Semiconductors before 2006. In 2006, the company was sold by Philips to private equity investors. The headquarters is in Eindhoven, the Netherlands. Now NXP is spread in more than 25 countries, with engineering design teams in 19 locations worldwide and it has 11 manufacturing sites, with six test and assembly sites and six wafer labs.

NXP is mainly produce some semiconductors which are based on some technology such as RF, analog, power management, interface, security and digital processing expertise. They are used in automobile, in vehicle networking, smart identification, wireless infrastructure, lighting, mobile phones, digital TVs, portable music players and computing applications and so on.

NXP is the co-inventor of near field communication (NFC) technology which enable mobile phones to be used to pay for goods, and store and exchange data securely, it increase the development of electronic transactions. NXP is the top 1 supplier for the chips which are used in government applications; number one in transport and access management, with the chip set and contactless card for MIFARE used by many major public transit systems worldwide; and is number one in RFID tags and labels.

Furthermore, NXP is the global market leader in many other areas, such as automotive chips for in-vehicle networking, passive keyless entry and immobilization, and car radios, as well as silicon tuners for the TV and set-top-box market. For in vehicle networking, NXP is the bellwether, these chips are used as interface between a microcontroller and a network. There are three general network systems, CAN (Controller area network) and LIN(local interconnect network) and Flexray (high speed).

Brands that are using NXP chips are e.g. Daimler-Craysia (Mercedes), Volkswagen, Audi.
1.1.2 Assignment background

There are a small number of failing products (two kinds of failures. one is application failure, for example, when people give pins excessive voltage; another one is production failure, before products are sold there must be some test to ensure they can work, but sometimes the test cannot cover full-scale, which leads to unqualified products) at customers. These customers buy some NXP products by wholesale, for example some automotive companies. The product can be any products of NXP which have pins for example, some devices or some chips of automobile. Figure 1 is Lin transceiver (TJA 1020), it is a NXP chip which used in automobile.

Products that are sent back to NXP will be handled by the Customer complain group. There are three kind of complains: Line-reject, 0 km-reject and Field-reject.

Line reject fail means that the chip is failing on the module, the module manufacture is doing a final test after assembly and the unit is not working correctly.

0 km-reject means that the product is failing when the assembled car is tested, this is done at the care manufacture so he will replace the module and send this back to the module manufacture.

Field-reject means that the car has a mail function and the car owner has to call for maintenance.

The defect products are sent back by customers for analyses in NXP laboratory, in this laboratory it is possible which of the many components in the chip is failing. Unfortunately customers are also sending products back that are working correctly, NXP call these products No Trouble Found (NTF).

Analyzing products is very expensive, so it’s a cost saving if we can avoid that customers send in good product. To achieve this, NXP has to give the customer a tool to do a first check of the device, curve tracing will give an idea of the condition to do the first check.

To minimize the cost, NXP wants to develop a standalone curve tracer for remote customers assist. The customers can test and get the V/I graph without help from NXP side. Then compare the graph with the reference. If the product has some problem, they will send the report and the defect products to NXP, the NXP site will analyze the defect products.

Curve tracing is one of the analyzing methods used by NXP. The objective of curve tracing is to measure the ESD protection each pin. Curve tracing is done by sourcing the voltage and measuring the current. The results are displayed in the V/I graph and compared with a reference curve, any abnormality of the defect product is now easy to see. There is already
curve trace equipment in the market, but curve trace equipment can be big, inefficient and not dedicated for NXP products. The device should also be easy to use, it should be a tool and display the results on a PC screen. And it is time-saving by the dynamic curve tracing, it just needs a short span of time to finish the testing. All products should be tested by the curve tracer, especially transceivers. Consequently the first step is to figure out the inner structure of the DUT and seek out their common features. Under these circumstances, the datasheets of basic LIN/CAN transceivers (TJA 1020/1040/1041) should be studied well.

Figure 2 is the ESD protection of a chip. A modern silicon chip is made in MOS (Metal oxide semiconductor), MOS components are very sensitive for ESD (Electro Static Discharge). To protect the components, every pin of the device has an ESD protection, mostly it will be a high speed zener diode.

Also every pin will have a certain behavior, e.g. an input pin will be high ohmic, maybe internal a pull-up or down resistor, which can avoid the pins with floating. Besides, in electrical circuits, parasitic capacitance is an unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit simply because of their proximity to each other. All actual circuit elements such as inductors, diodes, and transistors have internal capacitance, which can cause their behavior to depart from that of 'ideal' circuit elements. Additionally, there is always non-zero capacitance between any two conductors; this can be significant at higher frequencies with closely spaced conductors, such as wires or printed circuit board traces. Among the design, the characteristics of parasitic capacitance and the limits of voltage or current also need to make clear.

If the customer has a suspicious device and he will curve trace all pins and compare that with a reference device then he has an idea of the condition if it. For example if a pin is damaged because of electrical overstress (too high voltage on the pin) then the curve will show that.

Figure 2: ESD protection (Vishay Siliconix, 2008)
1.2 Research goal

In this section, the research goal would be described.

The aim of the assignment is to design a PC curve tracer to source the voltage and measure the current to replace the existing heavy curve tracer equipment.
1) The curve tracer need to be small enough and portable;
2) The measuring speed should be guaranteed;
3) The test results in PC screen should be distinct and readable enough;
4) The accuracy should be guaranteed in a certain range;
5) The budget should be taken into consideration.

1.3 Research Questions

In this section, the main question will be created first based on the background and the research goal. Then all the sub-question will be created and all the sub-question will be in accordance with the design method.

1.3.1 Main question

From section 1.1 and 1.2, after the analysis of the demands, the main question shows below:

Main question: How to build a portable PC curve tracer for customers to do the V/I curve tracing for testing DUT by themselves so that the company can cut down expenses and save time?

Specific: This project will be performed at NXP Semiconductors the Netherlands (Nijmegen). The failing products will be recovered from customers by the company. The curve tracing is supported by the relevant knowledge of software and hardware in the lab of the company.

Measurable: The device will be delivered. The test report will support it.

Assignable: The project will be finished by Xiaojing Yu. The in-company mentor and the school supervisory teacher are responsible for the guidance to help the project go on well.

Realistic: All the relevant technology are available. So it is possible to finish the project by combining them together and the final product with the program will be delivered.

Time-related: All the work will be finished at the end of June, 2015, but it is also acceptable before the end of August.

According to the above information, it shows the main question is specific, measurable, assignable, realistic and time-related. In this report, the main question is the core for every part.
1.3.2 Sub questions

The main question can be divided into some sub-questions according to the different parts of the design method (DDM). There are 5 phases, and sub-questions are divided into 5 phases below.

Analysis phase:
- What is curve tracing?
- What should be the functions and requirements of the device?
- How to make the curve tracer portable?
- What is ESD protection?
- What is parasitic capacitance?
- How to distinguish the different categories and the electrical characteristics of DUT pins?
- How to analyze the curve tracing? Some details analyzed by parameter, graph and diagram?
- What is the general voltage that should be provided to the device?

Idea phase:
- What functions of the software for FPGA should achieve?
- What functions should be achieved by the hardware?
- What should be devoted to man-machine interface?
- How to make the tracing speed quicker?

Concept phase:
- What is the best choice of connections (USB-provided by company) between PC and the device?
- What’s the best choice to achieve the voltage generating and controlling by programming?
- How to simplify the designs to reduce the cost under the situation of functions guaranteeing?

Materialization phase:
- What are the components need to be bought in market?
- What are the design rules of the PCB layout?
- How to achieve the design of the cabinet in material? Or just chose one cabinet from company?

Detailing phase:
- How to achieve all the software functions by program for FPGA?
- How to test if the curve tracer works normally and fulfill the requirements?
2. Theoretical framework

In this chapter, the research is about the theoretical knowledge of the curve tracer. It is helpful for knowing the principle and definition of every parts of the project. During the starting point of the concept phase, more research will be done related to the function and the solution to the requirements.

2.1 The significant concepts and relationships

In this section, 9 significant concepts will be listed based on the sub-questions. Afterwards, the relationship between them will display in a Figure 3, which makes the relationship readily comprehensible.

2.1.1 The significant concepts

Following are 9 significant concepts, the 9 concepts constitute the knowledge of the whole project. They are the foundation of this project.

- The knowledge of curve tracing
- The measurement method of the curve tracer
- The knowledge of DUT pins in transceivers and the ESD protection
- The knowledge of voltage generating and controlling
- The knowledge of schematic circuit design
- The knowledge of FPGA
- The knowledge of programming
- The knowledge of PCB board
- The knowledge of man-machine interaction

2.1.2 The relationship among concepts

The theoretical framework graphic can reflect the relationship among the significant concepts. Figure 3 below shows the relationship between them.

Firstly, the research of DUT, ESD protection is to set restrict and detailed demands for the design (including the voltage). Secondly, the research of generating and controlling the voltage is also necessary. FPGA is same as the brain of human-beings, Also, the program for FPGA is same as the memory storage of brain. After that, the schematic circuit should be designed and simulated by software. After the confirmation for the design of the schematic, PCB layout also need to be achieved. Then factory will produce the PCB board. A cabinet is also needed to be designed or selected. Furthermore, there must be connections between PC and PCB board, DUT
and PCB board. Finally the curve tracing process needs to be operated and controlled, since man-machine interface need to be designed and programmed.

Figure 3: The relationship among concepts

2.2 The explanation of concepts

- Curve tracing research
Curve tracer is an instrument to analyze characteristics of semiconductor, for example diodes, transistors and MOSFET’s. Usually the characteristics (relation between voltage and current) of components can display on an oscilloscope. Figure 4 shows the curve on an oscilloscope.

Figure 4: The V/I curve on oscilloscope
On this oscilloscope the relation V-I is connected to channels of the oscilloscope. The scoop needs dual channel so Ch1 is Y-axis and Ch2 is X-axis. The current is converted to a voltage via a resistor.

This project will also be a curve tracer but with other requirements than already existing and available on the market curve tracers. The method to measure the curve is in the same way as other curve tracers, apply a voltage and measure the current through the device. As shown in the Figure 5, a voltage Vs applied to a diode with in series the resistor, if ramp up the voltage Vs then the voltage over the diode and resistor is measured and displayed in a graphic.

![Figure 5: The curve tracing of diode](image)

- The Research of DUT, ESD protection:
  DUT:
  DUT means device under test, it is a device that is tested to determine performance. Figure 6 shows the testing PCB board and DUT. In this picture, DUT is the small board in the middle.

![Figure 6: The testing DUT](image)

The curve trace in this project will test several types of integrated circuits of NXP, mostly transceivers. The mean is that every pin is characterized, with a VI measurement and the outcome will be compared with an expectation of these characteristic. To create a measurement we need to know what is inside the circuit so we can predict how the VI curve will be. As example we have a look to the TJA1020, this is an NXP LIN transceiver.
As figure 7 and figure 8 show, there are 8 pins of TJA 1020—RXD, NSLP, NWAKE, TXD, INH, BAT, LIN and GND. Figure 9 shows the inner structure of TXD, a V/I curve will get as Figure 5 shows, step by step, all the pins need to analyze by the rule.

ESD:
ESD means Electro-Static Discharge, it is the sudden flow of electricity when two charged objects contact each other, it also can be caused by an electrical short or dielectric breakdown. There are two main test models for ESD tests: the human body model (HBM) and the machine model (MM). HBM is from human-beings, MM is from an object to the component.

Human Body Model:
Figure 10 is ESD-HMM test setup, when people get charged (e.g. by walking) and approach to the components, they build up energy will discharge via the component. Every step builds up charge that the equation is: $\Delta V = m \times \Delta q / C_p$ [1]
From formula [1], \( m \) is the number of steps per second and \( C_p \) is the capacitance of body. Assume steps on an insulating floor, \( \Delta V \) raise of 300 V per human step and reaching about 3 kV in 10 seconds.

Figure 10: ESD-HMM test setup

Here TXD is also used for an example, in the circuit of TJA 1020, if the voltage is too high, the diode will reach to the breakdown voltage and absorb the energy. The very high ohmic gate of the MOSFET of TXD is now protected. Without ESD protection, the gate of the MOSFET will get a dielectric breakdown.

Machine model:
Instead of a body described now charge from an object, also for this there is a test setup. MM is designed to simulate a machine discharging through a device to ground. The mode is same as in HBM testing. In the test setup, high-voltage supply with a resistor charges a capacitor from object. The switch represents when an object is close to the DUT and connects the voltage supply to the inductor for discharging. The inductor produces an oscillatory current waveform. Figure 11 shows ESD-MM test setup.

MM uses the same basic test circuit as HBM, but \( R = 0 \ \Omega \) and \( C \) is higher reach to 200 pF, which represents a Non-insulated object and it is used with a 1-M\( \Omega \) resistor for charging. The inductor is for discharging. (Agarwal, 2014)
To measure a V/I curve, a simple voltage sweep and measuring the current during that sweep is suitable, so a simple DC measurement is needed. However, a DC measurement will take a lot of time, a voltage need to apply and wait until it is suitable and measure the current. For a sweep from -5V to 15V with 1 mv/step, 20000 steps is necessary. With a measuring time of 2ms/step is will take 40 seconds, so a device with a pin count of 8(8×7 measurements) needs wait around 47 minutes to measure.

Another solution is to do the measurement dynamic, so it needs to sweep the voltage with an AC signal and sample the current via an AD converter. Problem with AC is that parasitic capacitors will influence the measurements because it will have a resistance. The parasitic capacitors in MOSFET can be seen in Figure 12.

But if keep the frequency low then these resistance will be big according to the formula [2]:

\[
X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \quad [2]
\]

If the \(X_C\) is big in the case of fixed voltage, the current of parasitic capacitors will be negligible so the measurement will not be influenced. So if choose 50Hz for the sweep then one measurement will take \(t = 1/f = 20mS\). The total time will now be \(7 \times 8 \times 20 \text{ ms}=1.12 \text{ S}\). This measurement is less accurate but if there is an abnormality then for that pin a DC sweep can be executed.

\[
\text{Figure 11: ESD-MM test setup}
\]

\[
\text{Figure 12: The MOSFET and its parasitic capacitances (Caka, 2007)}
\]

* The Research of generating and controlling voltage Signal Generator:

A signal generator is a device that can generate electronic signals e.g. sine, triangle, square, or burst waves. They are usually used for designing, testing, troubleshooting, and maintenance of electronic circuits. For this project, only triangle wave is needed so it needs a dedicated circuit as signal generator.

To achieve the voltage generating, signal generator is needed. Also, the ADC, DAC are also needed for the voltage information transmission between the computer and the curve tracer.
ADC (Analog-to-Digital Converter) and DAC (Digital-to-Analog converter):
In Figure 13, an ADC converter transforms an analog signal to a digital signal by sampling the analog signal. The digital output is an amount of bits that represent the amplitude of the analog signal. The information of the analog signal between the samples is lost so not only the amount of bits but also the sample frequency is determining the accuracy of the measurement. DAC performs the opposite function with ADC, digital data is converted to an analog signal, also here the amount of bits and conversion frequency will determine the accuracy.

![Figure 13: Digital control system with analog I/O](image)

(Kuphaldt, 2014)

- The research of Schematic circuit design & PCB board
  To design this project Altium designer will be used, with the help of the software tool schematics can be drew and Altium can run simulations and designing the printed circuit board. Also designing a FPGA project is possible in Altium designer.
  Altium Designer has some different project types. In this project, PCB project, FPGA project and Embedded project will be built. PCB project will help to draw schematic, build and run simulation model and wire PCB layout. FPGA project is used to configure FPGA hardware models. Embedded project will be allocated to FPGA project thus the C program in Embedded project can realize some needed functions.
  Simulation is important for the design, the circuit can be separated part by part to demonstrate if the voltage waveform is what needed or if it fits the theory. (Aldec FPGA simulation added to Altium Designer, 2010)

  The above research are all about the hardware design, after finishing the principle design, the programming part can start, the following are the research related to programming part.

- The research of FPGA and FPGA programming
  FPGA means Field-Programmable Gate Array; it is a configurable digital device so the requirements are determined by the content of the FPGA.
  In most FPGAs contains logic blocks e.g., memory elements, Flip-flops, some types of FPGA’s are also containing microcontroller cores.
FPGA’s are programmed with VHDL to describe the digital behavior, if embedded microcontrollers or hardcore microcontrollers are used then it will be done in C or C++. (Thompson, 2007)

In this project, Altium Designer has the FPGA project, and there are some modules in the library, these modules were made by hardware description language (VHDL). For this project, just need to study these existing modules, connect and configure them, finally use C program to achieve the needed functions.

- The research of HMI (human machine interface):
  A human machine interface (HMI), also called user interface is an interface between a human-being and a machine. Human machine interfaces should be functional, accessible, logical and give a good user's experience. Also, the human machine interfaces can be customized and developed by professionals according to the specific demands of the product. There are two parts in a HMI, input and output. Input is to make requests or control to the machine, such as switches, mice, keyboard and push buttons; Output is to make sure users can get the updated results along with the changing of the input, information gathered from PC screen or some other behaviors. (Ravi, 2009)
3. Method

In this chapter, the content of the design method will be described, after that would judge why the method is adapt to this project.

3.1 Introduction to Delft design method

The general approach of the project is strongly linked to the Delft Design Method (DDM). This methodology is commonly used for industrial design but with small modification it could also be used in designing an information system since this methodology has been studied systematically. DDM contains different steps that give a good directive to solve design tasks. In Table 1 shows the different steps of the method are written down.

<table>
<thead>
<tr>
<th>Delft Design Method</th>
<th>Activities</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analysis Phase</td>
<td>Research on topics</td>
</tr>
<tr>
<td></td>
<td>Introduction of background(company, assignment)</td>
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<tr>
<td></td>
<td>EDS</td>
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<tr>
<td>Ideas Phase</td>
<td>Idea development</td>
</tr>
<tr>
<td>Concept Phase</td>
<td>Concept development</td>
</tr>
<tr>
<td>Materialization Phase</td>
<td>Product development, Start Production, Development</td>
</tr>
<tr>
<td>Detailing Phase</td>
<td>Testing, Product optimization, Production development</td>
</tr>
</tbody>
</table>

Table 1: Delft design method
Figure 14 is the Model of the Product Innovation Process. It is also can be used in DDM. The analysis phase is about transferring customers’ requirements into Engineering Design Specifications (EDS), which will be important used for examining whether the whole project is proceeded in a right way or not. The ideas phase shows some ideas for each sub functions from function tree. Also need some explanations for every idea. Concept phase is the process of setting up concepts and evaluation for choosing the best concept among several concepts based on the Engineering Design Specifications (EDS) and the research. In the materialization phase, some parameters will be decided, design prototype (in this project should be the schematic and PCB board) will be built up and lots of test will be done by the guide of test plan until the test result is satisfied. The detailing phase is the phase to optimize the prototype. After that, it will make conclusions or the summary of the project. (Buijs and Valkenburg, 2005, 3rd ed.)

3.2 Justification

The Delft Design Methodology is suitable for this project. The reason is that all the sub questions and the main question in the thesis project can be solved one by one during these phases in DDM. And DDM pays more attention on analysis phase and concept design phase. Concept phase starts with considering the requirements of the PC curve tracer then discuss the different parts and concepts and finally mark the concepts in the argument of EDS. In this
project, the voltage generator part, cabinet design, switch choices and some components are uncertain parts which have several possible principles and concepts. It will be easier to choose these concepts with the help of Delft Design Method.

Delft Design Method has a rule of iteration work. The method stipulates that if a fatal problem is occurred in a phase, then the iteration work should be done at the last phase as a remedy. This work can prevent from missing. In this project, it can prevent the design of the signal generator (if the practical test is not accurate as the simulation one) and some components are not suitable for satisfying the circuit or the actual voltage testing is not that ideal. Then the iteration must be taken if that happens. Also, unexpected errors are also possible happens, all of them needs the iteration rules of Delft Design Method.

Taking all the information into consideration, Delft Design Method is chosen as the design method in this project.

4. Results

After the research, some design of this project would start. This chapter has 5 phase based on the design method flow. Pass through this chapter, all the outcome of the project would display.

4.1 Analysis phase

In this Chapter, the requirements and the related EDS were listed. The reasons for these EDS will also be given. The function and the sub functions were listed in a function tree.

This part is mainly discussed about the hardware and software parts, the program part will have a separate part to elaborate.

4.1.1 Engineering Design Specifications (EDS)

This part was according to the aim of project to formulate. The aim of project was in the 1.2 section (research goal), this also the requirements from the company. According to the requirements, the detailed EDS listed in Table 2. Also, the criterions also listed in this chart, leading to the relation with concepts part.

From the EDS chart, all the relevant requirements were mentioned. Thus the function of the PC curve tracer can be designed.
### Criteria for EDS

#### Functional requirements to EDS

**Generating the voltage** The voltage should be in the range of ±15V to ensure all the pins can reach appropriate voltage, their working voltage, and the current should be around 2mA.

**Quick measurement speed** The time to measure all the pins of DUT should be as short as possible.

**High reliability and accuracy** 1> The accurate rate (to test the broken pins) should be more than 95%; 2> There should also have a static voltage to confirm the failing pins; 3> Should have the appropriate method to achieve the noise reduction.

**High automation** 1> All the necessary elements of graph should be included and should be clear enough. Most importantly, the graph should generate automatically; 2> The voltage should be dynamic, can be from -15V to +15V in a certain period of time, then can achieve test all pins automatically.

**High flexibility** The power supply should be flexible to fulfill the demand voltage.

#### Dimensional requirements to EDS

**Small size** 1> The components should be not too big so that the PCB board can be smaller; 2> The curve tracer needs to be small and portable, the size of the cabinet should be smaller than 200mm*100mm*50mm

#### Budget requirements to EDS

**Low cost** The budget should be less than 1000 euros

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generating the voltage</td>
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</tr>
<tr>
<td></td>
<td>period of time, then can achieve test all pins automatically.</td>
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</tr>
<tr>
<td></td>
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</tr>
<tr>
<td></td>
<td>should be smaller than 200mm<em>100mm</em>50mm</td>
</tr>
<tr>
<td>Low cost</td>
<td>The budget should be less than 1000 euros</td>
</tr>
</tbody>
</table>

**Table 2: EDS**

### 4.2 Ideas phase

Altium Designer 15.0 was used as a tool to design the schematic circuit diagram, simulation and the PCB layout, for the schematic circuit diagram design, the design process, the components and their models, footprints, they were all displayed in a PCB board. It is called hardware designing.

In this section, the hardware design will be separated as several parts, on the basis of the requirements functions will be described in the function tree diagram. According to the functions, there will be some diverse selected objects. Besides, some explanation will describe the different objects to make them distinct. Whereafter, the Morphological Chart will assist to generate different concepts. The Weighted Rating Matrix was a vital evidence to evaluate concepts, the above process was the way to select the best concept.
4.2.1 Function tree

At the beginning of the project, the clues we have are the requirements. A diagram should first be built to show the desired functions and some determined parts, together with their relationship.

To build such a diagram, all the desired functions were listed first. After such a work, there was a diagram that shows the main function and sub functions. Such a diagram was called function tree. All the functions were listed in this diagram (can be found in Figure 15).

---

**Figure 15: Function tree**

The main aim of the device is to trace the V/I curve of the DUT. In order to realize the main function, three sub-functions have been found out: Testing, Analyzing the problem and Being portable.

For the sub function of Testing, the curve tracer can source the voltage and measure the current of the each pin of the DUT automatically and the value should be at the range of -15V to +15V. Firstly it needs power supply, the measurement should have a high speed and accurate. So it
needs the dynamic voltage (with proper frequency) to speed up the measurement and static voltage to make the measurement accurate.

For the sub function of Analyzing the problem, there should be a way to show the result of the measurement, then the graph should be generated on PC screen automatically and users can compare it with the reference graph.

For the sub function of Being portable, a cabinet should be designed to contain the PCB board. The main aim of the device was to trace the V/I curve of the DUT, In order to realize the main function, three sub-functions have been found out: testing, Analyzing the problem and Being portable.

4.2.2 Ideas

According to all the sub-questions from function tree, some ideas were listed and explained in Appendix 1.

Every sub-function has several ideas. The names and pictures of these ideas are also in the chart, at the right row of the pictures, there is explanation for every idea. Also, the concept phase is based on these ideas. The explanations in Appendix 1 helped every concept more clear and understandable.

4.3 Concepts phase

In this section, 2 concepts were created by the help of ideas for sub functions, some explanations were under every concept generation. After that, the criteria for concept judged the best concept.

4.3.1 Concepts generation

In this section, there are some general descriptions for the concept generation and choice. Firstly, the Morphological Chart (see from Appendix 2) was a method to generate concepts in an analytical and systematic manner. Through this Figure 16, different concepts will be generated.

The following is the 2 selected concepts, the ideas are all from Table 3, some explanations can be found.

Concept1: Power supply—Crystal oscillator, counter and DAC—Solid state relay—FPGA—Increasing the precision of ADC and DAC—Downloading a V/I curve tracer user interface online—Checking reference—Designing a cabinet—connecters
Figure 16: Concept 1 design diagram

This concept is tended to digital electronic design. The signal from crystal oscillator transported to counter, then the counter accepts the signal to achieve the counting function. Then DAC converts the digital signals to analog signals, then the triangle waveform can be created. From Table 2- Idea 2, some explanation about how it works.

By checking the datasheet of counter and DAC, the period time of the triangle waveform and the voltage value can be set; FPGA as a controller to manipulate DAC and ADC. After that, a downing V/I curve tracer interface will be used as an analyzed interface to display the graph, then users can check the datasheet of DUT and find the reference graph of the pin. Cabinet and connectors do not show in Figure 16, it just showed some visible functions hardware.

Concept2 : Power supply—Amplifiers with voltage divider—Multiplexer—NE555 (Timer IC)—Designing a static circuit— Programming a user interface—Instructions— An existing cabinet—cables

Figure 17: Concept 2 design diagram
Concept 2 is tended to analog electronic design. The circuit centres on NE555 timer, it needs some components, which produced some inescapable noise. Another important part of concept 2 is the static circuit. From the Figure 17, there should be a switch to convert the two models optionally, here the circuit centres on NE555 timer called dynamic circuit. Because NE555 circuit will generate 0~5V dynamic voltage, then the static circuit also should generate the voltage 0~5V static voltage, so DAC can generate DC voltage (static voltage). And the concept would have an exciting cabinet, cables connect with PCB board then come out of cabinet, so the DUT placement would be more flexible.

4.3.2 Concepts evaluation

From the Weight Rating Table (see from Appendix 3), the method can be explained by the below formula:

\[
\text{Source} = \sum Weight \times \text{Rating},
\]

On the basis of the formula, the two concepts were evaluated by scoring. From Appendix 3, concept 1 got a 2.95 score as concept 2 is 3.55. Obviously, concept 2 is the best concept.

The voltage generating way of concept 2 needs some analog components. Therefore, it will generate some components noise so that lead to unstable wave. But in consideration of the small impact, concept 2 is more abstract for starting a project and NE555 is cheaper. The plan of this project was delivering a hardware design then software design. Analyzing concept the voltage generating of concept 1 will be more abstract and complex since hardware and software design need to be take into consideration at the same time. Comparing the concept 1 and concept 2, there was three existing, alternative parts—user interface, cabinet and reference part. Concept 2 has the better choices. A customized user interface was suitable for the curve tracer of this project, which can expunge some needless and miscellaneous elements. For the cabinet, the purpose was to decrease the size of the PC curve tracer, at this situation, finding a proper and small enough cabinet is good enough. In addition, it decreased the expenditure of the project (It is expensive to design a customized cabinet without mass production). For the reference, in view of providing convenience for customers instruction was necessary, at least, sorting out different characteristics of graph reference.

4.3.3 The explanation of the best concept

From Figure 17 was the design process of the best concept. Some details about the concept should also describe. There should be a switch to change the two models, dynamic model should be the first step for measurement. After a rough measurement by dynamic model, the static model will run to be sure the problem. Then get the V/I graph of the failing pin. The dynamic model will use a NE555 to get a 5V square wave signal as the Static model generates the 0~5V
DC voltage. SMU was to source the voltage, here this SMU was changing the value of voltage to the demanding voltage and transfer the square wave to triangle wave, MUX controls which pin was under measuring. For example, the MUX controls the Pin 1 and Pin 4, then the measured voltage was the voltage between Pin 1 and Pin 4, ADC2 will transfer the analog signal to digital signal. At the same time, according to the ohm's law, when the current from DUT (the current from pin 1 and Pin 4) go through the Rsense, it can generate a voltage in Rsense. I/V converter will sense the instant voltage to current. Finally, the V/I graph will display on the PC screen.

4.4 Materialization Phase

In this section, according to the flow process diagram in last chapter, the entire PCB board will be designed. Two parts will have interpretation, the schematic part and the PCB layout part. After that, the hardware design will finish. There was a relative change of the project. The DAC and ADC has the voltage range, the plan A was that solder the FPGA and ADC, DAC in the PCB board (NB3000AL.02), considering the schedule and the difficulty of PCB layout of FPGA. The plan B used an Altium NanoBoard (shows in Figure 18) to make use of the DAC (DAC084S085), ADC (ADC084S021) and FPGA memory.

![Alitum Designer Development Board NB3000AL.02](image)

The ADC and DAC are both 4-channel, 8-bit devices. They are powered from a regulated 3.3V power supply, obtained by passing the motherboard's 5V supply. (Altium, 2013) The principle of operation was explained in the Chapter 2.
4.4.1 Schematic

From the best concept, some details were added in the diagram on the basis of Figure 19 as it described in section 4.3.3, it made the schematic design more unambiguous. Also, the schematic design followed Figure 19. 7 parts explained step-by-step below. During the schematic design, components choices also need to take into consideration.

![Diagram](image)

Figure 19: The design diagram of the best concept

In the process of designing the schematic diagram, the components’ type and model should be fit for the PCB board. It was also the concept part.

There are two types of Mounting in semiconductors, Through Hole Mounting and Surface Mounting:

Through Hole Mounting: Hence the name, this method will make the components go through in a multilayer PCB, it can work in the high voltage environment. See from Figure 20.

![Resistors](image)

Figure 20: Through Hole Mounting resistors
(Resistors SMD Leadform Option, 2014)

Surface Mounting: It has small size, light weight than the Through Hole Mounting components. In this method, leads are soldered on PCB surface directly rather than using double-sided installed. See from Figure 21.
Comparing the two types and considering the demanding voltage was not too high, so SMD was a better choice for this project.

Dynamic model and Static model were designed in this project for generating voltage. The detailed explanation will be described respectively.

**Dynamic model**

As shown in Figure 22, the resistor connects the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor CT charges through RA and RB and then discharges through RB only. Therefore, the duty cycle was decided by the values of RA and RB.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level and the trigger-voltage level. As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.

![Figure 22: The simplified Schematic circuit design based on NE555](image)

23: Internal structure of NE555

Figure 22: The simplified Schematic circuit design based on NE555

Figure 23 shows the internal structure of NE555. The operational principle of NE555 was described in Appendix 4.

The frequency and duty cycle can be calculated as follows:
The oscillation cycle is equals to the sum of duration of charging and discharging.
Charging time: \[ T_1 = (R_{A1} + R_{B1}) \times C_T \times \ln \left( \frac{V_{cc} - V_{cc}/3}{V_{cc} - 2V_{cc}/3} \right) = 0.693C_T(R_{A1} + R_{B1}) \] [3]

From formula [3] can get:

Discharging time: \[ T_2 = 0.693CR_{B1} \]

\[ T = 0.693 \frac{(R_{A1} + 2R_{B1})}{C_T} \]

\[ f = \frac{1}{T} = \frac{1.44 \times C_T}{R_{A1} + 2R_{B1}} \]

D = \( \frac{T_1}{(T_1 + T_2)} \) \times 100\% [4]

In formula [4], D means Duty cycle, it is the cycle of operation of a machine or other device which operates intermittently rather than continuously. The frequency needed is 50Hz, so \( T \) should be 0.02s, duty cycle should be infinitely close to 50\%. Then the general value can be calculated:

RA1= 1K

RB1= 43K

CT= 330nF (Texas Instruments, 1973)

These value were from simulation, firstly gave a approximate value, then tried to be tend to get the needed waveform.

Figure 24 shows typical waveforms generated during astable operation.
Figure 24: The simulation result of the generator

From Figure 24, the fold lines of trigger and output was shown, they have the net name in Figure 22, although trigger (pin 2) has the triangle wave, but it is not standard triangle wave. From the out (pin 3), the square wave is satisfactory, the cycle time is 20ms so that frequency is 50Hz. The simulation confirmed the calculation above. The output voltage is 5V with a 50% duty cycle and 50Hz frequency.

**Static Model**

Since the voltage range of DAC is from 0~3.3V, a circuit was designed to increase the voltage to 5V for matching the 5V dynamic model.

![Schematic of static model](imageURL)

The formula [5] of the noninverting amplifier is below:

\[
V_{out} = V_{in} \left( 1 + \frac{R_{T2-1} + R_{T2-2}}{R_{T1}} \right) = (0~3.3) \times \left( \frac{1.7}{3.3} \right) = 0V~5V \ [5]
\]

In Figure 25, the function of two jumpers (W1, W2) is a sustainable idea for the design, with the two jumpers, a 0~5V voltage range DAC (it can increase the accuracy) can be changed in the future. Also, the Nanoboard can be replaced by the DAC, ADC and FPGA chips. It will make the product more portable.
Switch:

Here is the switch TS5A63157 from Figure 26, Switch_IN will standby the switch, if it is Low level, the static model will conduct and if it is High level, the dynamic model will conduct.

<table>
<thead>
<tr>
<th>NO.</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NO</td>
<td>Normally open</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Digital ground</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>Normally closed</td>
</tr>
<tr>
<td>4</td>
<td>COM</td>
<td>Common</td>
</tr>
<tr>
<td>5</td>
<td>V+</td>
<td>Power supply</td>
</tr>
<tr>
<td>6</td>
<td>IN</td>
<td>Digital control to connect COM to NO or NC</td>
</tr>
</tbody>
</table>

FUNCTION TABLE

<table>
<thead>
<tr>
<th>IN</th>
<th>NC TO COM, COM TO NC</th>
<th>NO TO COM, COM TO NO</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>H</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

Figure 26: The schematic of switch

Figure 27: The pin description and function table of TS5A63157

(Texas Instruments, 2005)

SMU

SMU is a big part for the schematic design. First of all, the 0~5V square waveform was converted to -15~+15V square waveform. Secondly the -15~+15V square waveform was converted to -15~+15V triangle waveform.

In Figure 29, when it turns dynamic model, the 5V square wave signal enters through SMUIN, when it comes out, the 15V triangle wave signal generates.

In Figure 29, the function of the first op-amp U2 is to amplify the voltage from 5V to 15V, according to the formula,

Because the voltage from SMUIN is 0~5V, so the voltage range before U4 is -15V~+15V square wave.

The calculation process is below:
The negative electrode of the op-amp:
Gain1 = \frac{R_{3-1} + R_{3-2}}{R_2} = \frac{6}{1} = 6 \ [6]

So, from formula [6] the voltage range through this side is:

\((-15 \sim +15) \times 6 = (-30 \sim +30)V\)

The positive electrode of the op-amp:

Gain2 = \frac{R_3}{R_2} + 1 = \frac{7}{1} = 7 \ [7]

The voltage before the positive electrode: \(\frac{R_2}{R_2 + (R_{3-1} + R_{3-2})} = \frac{1}{6+1} \times 15 = -\frac{15}{7}V\ [8]\)

So, from formula [7] [8], the voltage range through this side is, \(-\frac{15}{7}V \times 7 = -15V\)

Finally the Vout is \((-30 \sim +30) + 15 = (-15 \sim +15)V\)

U4 is an integrator circuit.

From the circuit, in the normal integrator circuit,

Time constant: \(T = R_6 \times C_6 = 10K \times 0.47 \mu = 4.7ms < 20ms\) (square waveform width).

At this situation (RC is very small), the circle time of the triangle waveform is equal to square waveform.

R8 is the offset voltage of the op-amp U4, it is integral drift leakage resistance. It will charge and discharge capacity, the capacitor C6 is easy to be saturated. Usually \(Rf \geq 10R2;\)

R7 is a static balance resistor, it can compensate the imbalance by bias current. Usually \(R7=R6;\)

The process of the charge and discharge can be described by formula [9]:

\[V_{out} = \frac{1}{R_6C_6} \int V \text{mdt} \ [9]\]

For the RC circuit (Figure 28), the charging time should be at the range of 0~63\%RC, then a triangle waveform was formed, but also needs to output the demanding voltage (-15V~+15V).

With the increasing of \(C_6, R_6C_6\) (time constant) is increasing, as the circle time is 10 ms, so the capacitor value cannot be too big. For example, value \(C_6 = 50\mu\), the \(R_6C_6 = 50ms > 20ms\), so Vout cannot reach to ±15V. What is more, due to the amplifier is not ideal, the inside structure of U4 is unknown also too difficult for the bachelor level and the circuit also has the offset voltage, so the theoretical value was far away from the practical value. Therefore, the assist of simulator of Altium was necessary. After many times simulation, the value of the capacitor and R6 can be set.

![Figure 28: The charging process of a RC circuit](image-url)
Because R6 and C6 is shunt-wound, Then C will form a loop through R to discharge; Then the voltage across the RC is actually the alternate voltage during C discharging. Change the value of R6, the discharging time of C6 will also change at the same time.

Figure 29: Part of SMU schematic

Figure 30 is the simulation of the SMU circuit. Out1 is the 5V square wave from SMUIN, out2 is the amplifying ±15V square, out3 is the ±15V triangle wave. In Figure 30, for the triangle wave, the area of the charging and discharging time is same as the area of square wave.
Figure 30: The simulation of the SMU circuit

Figure 31 is the simulation of static model voltage. The voltage generated by DAC finally can be a static voltage from -15V~15V by the SMU process, then can do an accurate measurement of the abnormal pin. For example, the voltage measurement range can be set to 13V~15V to determine the failing pin.

● I/V converter
Since the result will display as a V/I graph form, but the circuit just provided voltage to DUT, so there should be a circuit to sense the feedback current.
From Figure 29, The voltage through R17 (Rsense) to SMUOUT, SMUOUT goes into the
MUX part, MUXs are controlled by programming open or close, finally DUT is provided the voltage, at the same time, the current from DUT gives a feedback to Rsense, the voltage range of ADC1 is 0~3.3V, so the voltage range of I/V converter is set to 0~3.3V (because the current range is -2mA~+2mA, when -2mA, it should reflect to 0V, similarly, when it is +2mA, it should reflect to 3.3V). So the according to the calculation, the value of RIN, Rout can be known.

From the datasheet of AD8227, the current range is ±2mA, considering the current maybe very big, some measurement should be taken to do the current limit. A 3mA current is considered a proper current limit.

AD8827 is bidirectional and has a suitable input voltage supply. Figure 33 showed 8 pins of AD8227, some information about the 8 pins can be found in datasheet. From Figure 32, the voltage rating is ±18V, so the maximum and minimum voltage is far more enough. Here set the supply voltage is ±15V, so the voltage input range is ±25V.

From the datasheet of AD8227, the transfer function of the AD8227 is:

\[ V_{out} = G \times (V_{IN+} - V_{IN-}) + V_{REF} \] [10]

Where: \( G = 5 + \frac{80K\Omega}{R_G} \) [11]

By approximate calculation and according to formule [10] [11], Rsense (R13) was set to 100Ω so that Vsense = (-2mA ~ +2mA) \times 100 = -200mV~+200mV. Also, assume \( R_G \) is 40KΩ, the G=7, the voltage range of ADC is 0~3.3V, so \( V_{out} \) is range from -1.4V ~ +1.4V without \( V_{REF} \). If \( V_{REF}=1.5V \), then \( V_{out} \) is range from +0.1V ~ +2.9V (this range is included in 0~3.3V).

UV circuit is to transfer the -15~+15V voltage to 0~3.3V voltage. So the function of the UV circuit can achieve by the amplifying circuit and the voltage divider. Finally, the voltage go through AD2 is from 0~3.3V. that is say, when AD2 receives a 0V voltage, the real voltage is -15V. similarly, when AD2 receives a 2V voltage, the real voltage is \( \frac{30}{3.3} \times 2 - 15 = 3.2V \). Also, 3.3 V matches with +15V.
As the above paragraph mentioned, a current limit (see from Figure 34, the circuit around U4) is needed to restrict the current. The voltage is 32V, so the value of R16 can calculate:

\[
\frac{32-2V_d}{I} = \frac{32-2\times0.7}{1\text{mA}} \approx 30\text{K}\Omega
\]

\(V_d\) is the voltage of each diode, so \(V_d = 0.7\text{V}\). Assuming the current I in R16 is 1mA, then can get the R16.

Q1 is PNP transistor, so the voltage in the transistor is 0.7V,

\[
R_{17} = \frac{V_{PD1}+V_{PD2}-V_{BE}}{I_1} = \frac{0.7+0.7-0.7}{3\text{mA}} = \frac{0.7+0.7-0.7}{3\text{mA}} \approx 233\Omega
\]

Because some components have no simulation models in Figure 34, so the current limit part was isolated in a project file with some components with simulation models, also provide the same voltage as Figure 34 shows. The schematic can be found in Figure 35.
For making sure the current is around 3mA, Figure 36 is the simulation of the current limit, after adjusting the resistance value of R17, the approximate was simulated at around -3.0027mA. At this condition, the value of R17 is 169Ω.
The ±15V voltage goes through the MUX to DUT, there should be 20 MUX, 10 of them connect with SMUOUT, the rest of 10 MUXs connect with GND (Ground). So there are 80 pins (every MUX has 8 pins connector) can be measured. In accordance with sequence, PA1 has 79 pins to conduct, PA2 has 78 pins to conduct…PA79 just can connect with PA80 and get the voltage between this two pins.

So, the time of dynamic model should be $80 \times 79 \times 20 \text{ms} = 126.4 \text{s} \approx 2 \text{ minutes}.$

As Figure 37 shows, MUX1, MUX2, MUX3…MUXK connect the EN of U6, U7, U8…U25 respectively. A0 connects with A0 of MUXs (from U6 to U15) in a series way. Similarly, A1 connects with A1 of MUXs, A2 connects with A2 of MUXs, A3 connects with A1 of MUXs (from U16-U25)…A5 connects with A5 of MUXs (from U16-U25).

Figure 38, Figure 39 are ADG5208 Pin function descriptions and truth table, which decide the design MUX schematic circuit.
These MUX are controlled by programming. Below is an example for controlling. If it needs to measure the voltage between PA 1 and PA 14, Firstly the EN of MUX1 and MUXC should be set to 1 (activated). By checking Figure 39, the digital signal of A2, A1, A0 should be 000, and the digital signal of A5, A4, A3 should be 101, then it generates a closed loop, so the instant voltage has a feedback to ADC1 and ADC2, finally generates the V/I graph.

- **Connection**

There should be some connection between DUT and the device, also between PC and the device. It is one part of the schematic design. Figure 40 and Figure 41 showed the headers P1, P2, P3, P4, P1 and P2 connect with the Altium Nanoboard, then Altium Nanoboard connects with PC by USB. P3 and P4 connect with DUT. It also defines each pin in headers for the programming so that we can control the test process of the curve tracer.
Since each pin of headers were defined, for example, in Figure 40, the Switch_IN is the enable of switch TSSA63157, ADC, DAC and MUXs also are controlled by programming, they were described in MUX section.

In figure 41, P3, P4 are headers to connect with DUT, 80 pins in all.

![Figure 40: Headers between PC and the device](image)

![Figure 41: Headers between DUT and the device](image)

With all the design finished, the whole schematic project shows in Appendix 5, in Appendix 5, firstly, a project file (curvetracer.PrjPcb) was set in Altium Designer. The schematic diagram was divided into several parts. The toplevel schematic (toplevel.SchDoc) was the integral schematic diagram, the rest of the sub schematic are under toplevel (generater.SchDoc, SMU.SchDoc, MUX.SchDoc). The toplevel schematic included all the sub schematic elements (the connected relations), and sub schematic included all the detailed information.

### 4.4.2 PCB layout

The PCB layout can be seen in Appendix 6, there are 6 layers in this PCB, TopLayer (Red wire), MidLayer 1 (yellow wire), MidLayer 2(bright blue wire), MideLayer 3 (purple wire), GND layer (green wire) and BottomLayer (dark blue).

There are several rules for the layout.

- The angle of wires should not be a 90° angle. If 90°, the current flowing in the 90° point is very large, will damage the wire.
- The thickness of wire is at least 10mil except power wire, because of the current in the circuit is not that big, so 15mil is thick enough.
- Capacitors should be as close as possible to the corresponding components.  The power supply, connectors should near the edge of the board.
4.5 Detailing phase

This phase will show some details of this project. The introduction of some procedures before sending the PCB to the manufacture needs to be explained. Some information about components and PCB board need to be distinct to PCB manufacturer. Programming for the device was necessary, C language was used in FPGA programming. Altium Designer 15 has its own build environment for FPGA so that C language can be recognized and compiled in Altium Designer 15.

4.5.1 Bill of materials

Before manufacture, there should be a list for components. It should at least including the components name in PCB, supply numbers so that the factory can buy the correct components and put the components to the right place. From Appendix 7, it was easy to find the matching of every component. What is more, It helps readers to understand the schematic well. Most of the components can be bought from Farnell, just the switch U2 needs to be bought in another company, Digi-Key. Workers cannot distinguish the PCB layout directly, so CAMtastic1 and CAMtastic2 were generated by selecting Gerber files. From Appendix 8, CAMtastic1 makes layers more clear and CAMtastic2, The position of holes can be seen clearly.

4.5.2 Programming

There were two parts needs program to run—FPGA (DAC, ADC and something else which introduced in previous section) and user interface. DAC programming was focused on in this section.

The FPGA program has been discussed in section 1.3.2. Before programing, FPGA hardware needs to be configured first.

The generation of the static voltage (from 0~3.3V); the switch U2, Switch_IN gives a low or high electrical level to control the on-off of NC or NO;

ADC1 and ADC2 gain the value of current and voltage respectively as a digital model;

MUX1, MUX2…MUXK will decide the on-off of each MUX;

A0, A1, A2, A3, A4, A5 will decide the on-off of S1 to S8, then can be accurate to control each pin in MUX;

According to the above information, the program should achieve controlling all the function.

- FPGA configuration

From the flow of the project, First of all, 0~3.3V voltage needs to be generated by the help of FPGA and DAC084S085, Altium Nanoboard 3000 was connected with the PC so that it can be simulated.
Firstly the dac084s085 FPGA project was built. The relationship between DAC and FPGA can be found in Appendix 9- dac084s085.SchDoc*. The green block in the diagram is the FPGA in Altium Nanoboard 3000. The FPGA is connected with DAC by SPI (serial peripheral interface) protocol.

From Figure 42, the red mark shows the DAC module, and it also shows the connection with FPGA. Also from the figure 42, there is a reset button in Nanoboard. So a OR logic can give the system a stop when it was running (namely the CLK_BRD gives the CLK constantly). Other configuration about FPGA and DAC can be seen in Appendix 9- dac084s085 System.OpenBus.

There is a processor in the OpenBus system, With Altium Designer, creation of soft processor-based systems, run within a chosen target FPGA device, becomes second nature - utilizing one of the many supported flavors of ‘soft’ 32-bit RISC processor, wired up to access peripheral I/O and memory over a standard bus interface.

Because the voltage generation process from DAC needs to be monitored, therefore, a terminal is necessary. It served as a temporary interface. I/O of processor connected with SPI master controller and SOFT_TERMINAL (signal harnesses) through a peripheral. The SRAM memory is necessary to configure, ISSIIS61LV25616AL is a proper memory chip to store data.

![Figure 42: The details in the dac084s085.SchDoc*](image)

**DAC programming**

After the configuration, an embedded project was built in this FPGA project. It is includes a C program (It can be found in Appendix 10-main.c) and a platform which is imported from FPGA. As it shows in Figure 44, only all the files are ready in this project and connect the Altium Nanoboard 3000 with computer by USB 2.0, then click on “Open the device view page”, the view page will show and the status displays “connected”. The view page is in Appendix 11, it needs compile, synthesize, build and program FPGA, in the red mark area of Appendix 11, the configuration of FPGA hardware and software will be downloaded in the FPGA chip. Then click on the “Terminal” (the green area in Appendix 11). The functions of C program will achieve in this Terminal (see from Figure 43). Also, voltage delivering process will display in the DC power monitor.
The realized function of C program (see from Appendix 10-main c) was generating continuous DC voltage (from 0-3.3V). Because the DAC is 8 bits, from the binary-to-decimal conversion, it should be \(2^8 - 1 = 255\), so each number will get \(\frac{3.3}{255} \approx 0.01294V\). There should be a start voltage ‘vs’ and a stop voltage ‘ve’ to define the range of voltage. After the testing of dynamic model, for example, the definite voltage range is between 1V~2V, then it can reduce the voltage range by setting vs =1V, ve=1.5V, If the graph shows same as the reference, then the range should be from 1.5V~2V (As Figure 43 shows, 1.5V is the start voltage and 2V is the stop voltage, 115 matches 1.5V, similarly 153 matches 2V). Follow these steps, the iffish voltage will be confirmed.

5. Discussion

In this chapter, there are 4 parts to do the discussion. Firstly is to analyze the result of chapter 4, secondly, it needs to compare the result and the original requirements from company then get the limitations of the project; Secondly, it needs to answer every sub-questions. Finally, the challenging and the difficulties of the project need to be discussed.

5.1 Result Overview

The device finally can generate -15~15V voltage in two model (dynamitic model and static model), and the current was limited to around 2mA. And the measuring time on each pin satisfied the requirement, each pin cost 20ms. Some capacitors near some components (for example, op-amp and MUXs) can reduce noise. The power supply is flexible enough, can adjust to the needful voltage. For small size, all the components are SMD model, and the PCB board design small enough (about 12cm*10cm).
About the accurate rate of the device, because of the time limit, the PCB board is not end of manufacture, so the testing cannot start. Therefore, the accurate rate is unknown. Also, the user interface is the vehicle of V/I graph. The user interface of this project is not start so that the graph cannot design and display. The cabinet was discussed in section 4.3.2, the cabinet of best concept was decided to choose an existing one, hence after everything is finished, a small and suitable cabinet will be chosen.

There were some challenges of this project. Some calculations needed the proof of simulation, also, for generating the PCB layout, every component needs their precise footprints so that the dimension can match the dimension of actual production. These tasks need much time to search for. Due to decrease errors of PCB layout, manual-routing took the replace of auto-routing, which took a lot of hours.

5.2 Answers of Sub questions

Analysis phase:

➢ What is curve tracing?
   As what is shown in section 2.2, there is curve tracing research.

➢ What kind of measurements should be used?
   According to the description of section 4.3.2 and 4.3.3, there are 2 concepts (the concepts are mainly about measurements). Finally, concept 2 is the best concept. There are two measurements method used in this project-dynamic model and static model.

➢ What should be the functions and requirements of the device?
   This question can be found in the section 4.1.1(EDS) and 4.2.1(function tree).

➢ How can make the curve tracer portable?
   Firstly, the size of the PCB board is limited. Also, from the best concept, a small cabinet should be chosen to make the curve tracer portable.

➢ What is ESD protection?
   The definition of ESD protection and three ESD test models are shown in section 2.2, the research of DUT, ESD protection.

➢ What is parasitic capacitance?
   The information about parasitic capacitance can be found in section 2.2. It is explained in ESD research, also including Figure 12: The MOSFET and its parasitic capacitances.

➢ How can we distinguish the different categories and the electrical characteristics of DUT pins?
   It needs to do the reference graph (checking the datasheet of the components characteristics and test the ideal components provided by company) in advance according to the components order from customers.

➢ How to analyze the curve tracing? Some details analyzed by parameter, graph and diagram?
This question is answered at the beginning of the project. The curve will be displayed on the PC screen. Then customers will compare the graph with the reference graph.

- What is the general voltage should be provided to the device? The voltage should be from -15V ~ +15V.

**Idea phase:**

- What functions of the software for FPGA should achieve?
  The functions of the software for FPGA are to generate voltage (by DAC) for the static model and receive the current and voltage feedback (by ADC) from DUT.

- What functions should be achieved by the hardware?
  The functions of the hardware can be found in Figure 15, should be one of the main function of the function tree-Testing. There are also some explanations below the function tree about the hardware.

- What should be devoted to man-machine interface?
  This question cannot answer, for the interface part is not started.

- How can make the tracing speed quicker?
  It is described in section 4.3 concept phase, NE555 is used for generating the triangle wave.

**Concept phase:**

- What is the best choice of connections (USB-provided by company) between PC and the device?
  From the introduction of section 4.4, some changes of the project are described. So PC connected with the device via the USB connection with Nanoboard.

- What’s the best choice to achieve the voltage generating and controlling by programming?
  The static voltage is generated by the DAC, it is controlled by the FPGA. It can be seen in section 2.2, the research of generating and controlling voltage.

- How to simplify the designs to reduce the cost under the situation of functions guaranteeing?
  Firstly, the area of the PCB board decreased, it can be seen from section 4.4.2. Secondly, the cabinet chose is an existing one, so it decreased some budget (a small order of cabinet will cost much money).

**Materialization phase:**

- What are the components need to be bought in market?
  The bills of materials were listed in Appendix 7, the name of components, quantity and the supplier number can be found.

- What are the design rules of the PCB layout?
  All the design tips of the PCB layout during the project are explained in section 4.4.2 PCB layout.

- How to achieve the design of the cabinet in material? Or just chose one cabinet from company?
Finally concept 2 is chosen as the final concept, a ready-made cabinet will be selected for the PCB board.

**Detailing phase:**
- How to achieve all the software functions by program for FPGA?
  
  C language is the programming language for FPGA, by configuring the FPGA hardware in Altium Designer and downloading it to FPGA in Nanoboard 3000, therefore all functions will be achieved.

- How to test if the curve tracer works normally and fulfill the requirements? It should have a testing phase in chapter 4, but the PCB board is still not be transported to company, so cannot do the test.

### 5.3 Method

In this project, the DDM design method was described and explained in Chapter 3. It was mentioned that one of the advantages of this method is idea and concepts choices, which helped to find a proper ideas for concepts and evaluated the best concept by the reasonable and scientific evaluation.

About the iteration work, firstly it was the application of Altium Nanoborad, it is the iteration work. Secondly it was in section 4.4, the factory did not have available component (the previous component, it was not shown in this report), so that the schematic and PCB layout had some alterations.

### 6. Conclusions & Recommendation

#### 6.1 Conclusions

The goal of the project is to build a portable PC curve tracer for customers to do the V/I curve tracing for testing DUT by themselves so that the company can cut down expenses and save time.

Firstly some research and analyzed the requirements were done to get some ideas for functions, secondly the best concept was chosen through 2 concepts.

The schematic design was the first step for the practical setup design. It is the mechanical part of the project. In this step, all the component models with their footprints were chosen. What is more, the connections with DUT and computer were named in each pin of the device. Also some needed waveforms were simulated in Altium Designer, which made the schematic authentic.

After the schematic design, to manufacture the setup, a PCB board was made through layout and wiring, which followed some PCB layout rules to make the board qualified to manufacture.
At the end, the DAC programming was made to generate voltage. Before programing, the FPGA hardware was configured. All the process also finished in Altium Designer, C language is the programing language.

Before starting the project, a schedule was made for the four months internship. But after several weeks working, it spent much time to study some design tools, software and gain some technical knowledge, also some calculations. So the company mentor did some changes of the project. The mechanical part and part of software were finished. But the rest of software part and the test phase will be done by the followers. After everything finishes, the device will be send to customers, then they will do test themselves, the company will save time and cut down expenses enormously.

### 6.2 Recommendation

In this section, some suggestion will be given to tell what should be done in the future and some other functions can be improved.

Limited to the time, this project needs to finish and improve afterwards. The rest of the software part (ADC programming and User interface) and the testing part need the following people to finish. For the followers, the following are the recommendation and suggestions.

1. All the connections (the name of every pin in headers and components) between hardware and software were marked in the schematic, next designer should check the schematic carefully and follow the existing name to setup parameters of C programming.
2. It is better to put the FPGA, DAC and ADC chips in the PCB board. Finally the cabinet will include every part of the device (leave out the Altium Nanoboard to make the device more portable).
3. The first step of testing should be the checking of the PCB board, to find if the device can work normally. Then ask some ideal DUT from NXP to do the reference graph, finally do the real testing to find out the problems of failing DUT.
4. Before writing the rest of the program, the followers should configure the FPGA hardware renewedly, add some modules for example ADC module.
References


Appendixes

Appendix 1:

<table>
<thead>
<tr>
<th>Functions</th>
<th>Ideas</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-function 1:</td>
<td>Idea 1: Battery</td>
<td>The battery can provide the fixed voltage.</td>
</tr>
<tr>
<td>Providing power</td>
<td>Idea 2: Power supply</td>
<td>The power supply can adjust voltage needed.</td>
</tr>
<tr>
<td></td>
<td>Idea 1: Amplifiers with voltage divider</td>
<td>This idea needs an AC voltage generator, then calculate the gain of amplifiers and the voltage divider part to get the needed voltage.</td>
</tr>
</tbody>
</table>
Generating the AC -15V~+15V voltage

Idea 2: Crystal oscillator, counter and DAC

The crystal oscillator handles the counter to send the signal to DAC.

\[ f = \frac{1}{2^{12}-1}, \quad T = 20\text{ms}, \quad \text{so} \quad f = \frac{1.96}{2^{12}-1} \]

Idea 1:

Normal analog switch:

The normal analog switch is the switching components, it can switch or route analog signals. It needs decoder to integrate all the switches to be a functional entirety.

Sub-function 3:
Testing the voltage current each pin automatically

Idea 2: Multiplexer

Multiplexer is also a kind of analog switch, but including the requisite decoder itself.

Idea 3: Solid state relay

SSR is an electronic switching device, small signal can control current and voltage. The speed is slower than analog switch.

Sub-function 4:
Quick measurement speed

Idea 1: NE555 (Timer IC)

Here, NE555 is used for AC signal generation, it generates a square wave.

---

<table>
<thead>
<tr>
<th>GND</th>
<th>1</th>
<th>OUT</th>
<th>3</th>
<th>TRIG</th>
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<td>7</td>
<td>DISCH</td>
<td>5</td>
<td>4</td>
<td>CONT</td>
<td></td>
</tr>
</tbody>
</table>

---
Idea 2: FPGA

Using a FPGA generates demanding AC signal.

Sub-function 5:
Measurement precision

Idea 1: low noise and high accuracy components
Choosing some components with low noise and high accuracy. Then can decrease the disturbance to the signal.

Idea 2: Increasing the precision of ADC and DAC

The ADC and DAC has the different bits, more bits means more accurate. For example, for 0-5V voltage, If it is 8 bit, the voltage can be accurate to 0.0195V, If it is 12 bits, it will reach to 0.0012V.

Idea 3: Designing a static circuit. After a dynamic measurement, circuit because it is a relative rough measurement, so it cannot reach the demanding precision

Sub-function 6: graph the PC

Idea 1: Programming a user interface
Writing the user interface by programming to adapt to this project, usually use the software Delphi.
**Generating the automatically on screen**

**Sub-function 7:**
Comparing the graph reference graph

- **Idea 1:** Checking datasheet
  - Users checked the characteristics of pins in datasheets of every component, then analyse the correct graph themselves.

- **Idea 2:** Instructions
  - Doing the ideal products graph reference and Sorting out all the reference and writing the instructions.

- **Idea 3:** Electronic document
  - Writing an electronic document (Access or Excel documents) so that users can find the reference handily and rapidly.

---

**Sub-function 8:**
Small size of cabinet contains the PCB board.

- **Idea 1:** Designing a cabinet
  - Designing a unique cabinet to contain the PCB board.
<table>
<thead>
<tr>
<th>Idea 1: Connectors</th>
<th>Using an embedded connectors and the open cabinet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idea 2: Cables</td>
<td>Using cables with the closed cabinet</td>
</tr>
</tbody>
</table>

**Sub-function 9:**
Connectors of the cabinet can connect the DUT, PCB board and PC

**Appendix 2: Morphological Chart**
### Appendix 3: EDS weighing table

<table>
<thead>
<tr>
<th>Subfunctions</th>
<th>Idea 1</th>
<th>Idea 2</th>
<th>Idea 3</th>
</tr>
</thead>
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<td>Generating the ±15V voltage</td>
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<td><img src="image" alt="Relay" /></td>
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<td>Testing the voltage and current each pin automatically</td>
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<td><img src="image" alt="Relay" /></td>
</tr>
<tr>
<td>Quick measurement speed</td>
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<tr>
<td>Measurement precision</td>
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<td><img src="image" alt="Resolution Chart" /></td>
<td><img src="image" alt="Graph" /></td>
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<tr>
<td>Generating the graph automatically on the PC screen:</td>
<td><img src="image" alt="Software Interface" /></td>
<td><img src="image" alt="Software Interface" /></td>
<td><img src="image" alt="Graph" /></td>
</tr>
<tr>
<td>Comparing the graph with the reference graph</td>
<td><img src="image" alt="Comparison" /></td>
<td><img src="image" alt="Comparison" /></td>
<td><img src="image" alt="Graph" /></td>
</tr>
</tbody>
</table>
Appendix 4: The operational function of NE555

Pin 8 is voltage input port, the voltage of Vcc is between 5~18V; from the circuit, Pin 5 is fixed on 2Vcc/3 as the Noninverting input of A2 is fixed on Vcc/3.

Pin 1 is ground, pin 2 is trigger input, pin 3 is output, the output level state is controlled by trigger. As well as, the trigger is controlled by the upper comparator and the under comparator. when trigger receives the High level of A1, the trigger will reset, pin 3 outputs Low level; pin 2 and pin 6 is complementary, pin 2 only takes effect on Low level, as when the voltage is lower than Vcc/3, pin 3 outputs High level.

pin 6 is threshold port, only takes effect on High level, as when input voltage is greater than 2Vcc/3, pin 3 outputs Low level (since the voltage of pin 2 has to be greater than Vcc/3). pin 4 is reset port, when the voltage of pin 4 is lower than 0.4V, pin 3 will output Low level no matter any states of pin 2 and pin 6.
Pin 5 is control port.
Pin 7 is called discharge port, it has a synchronous with pin 3, but no current.
Pin 8 is voltage input port, the voltage of Vcc is between 5~18V; from the circuit, Pin 5 is fixed on 2Vcc/3 as the non-inverting input of A2 is fixed on Vcc/3.

Appendix 5: Schematic
toplevel.SchDoc:
Appendix 6 : PCB layout
### Appendix 7: Bills of materials

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Appendix 9: The configuration of FPGA and DAC
dac084s085. SchDoc*
Appendix 10: dac084s085.PrjEmb

dac084s085.Swplatform:
main.c:
#include <stdlib.h>
#include <stdio.h>
#include <time.h>
#include <devices.h>
#include <timing.h>
#include <drv_dac084s085.h>

static void init( void );
dac084s085_t *dac;
volatile bool done;
char vs, ve [256];

/********************************************
| * | * Function : main
| * | * Parameters : None
| * | * Returns : None
*/ Description : Continuously write data to the selected DAC ports
*/

void main()
{
  clock_t t; uint8_t
  channels; int val = 0,
  direction = 1; int va;
  int cs=0,ce=0; int va_prev
  = -2; int more; double
  vs_a,ve_a; double vout=0;
  init();

  while (!done)
  {
    t = clock() + CLOCKS_PER_SEC / 10;

    dac084s085_write( dac, DAC084S085_OUTA, (uint8_t)val,
    1); va = val; vout = 3.3*va/255;
    vs_a = atof(vs); ve_a = atof(ve); cs=vs_a *
    255/3.3; ce=ve_a * 255/3.3;

    if (va != va_prev)
    {
      printf( "%2d: Write = %d, %f v\n", (int)(t / CLOCKS_PER_SEC), va,vout );
      va_prev = va;
    }

    while( clock() < t ) __nop();

    val = val +
    direction; if (val >
    ce)
    {
      val = ce;
      direction = -1;
    }
    if (val < cs)
    {
      val = cs;
      direction = 1;
    }
    if (val != 0 && ce != 0)
{   
    if(val == ce)  
        break;
   
}

/***************************************************************************/
/*
/* Function : init
/*
/* Parameters : None
/*
/* Returns : None
/*
/* Description : Initialize the hardware
*/
static void init( void )
{
    // Say hello to the user
    puts( "File '" __FILE__ "' compiled " __DATE__ ", " __TIME__ ");

    printf( "Input the start voltage: \n");  
    gets(vs);
    printf( "Input : %s\n",vs);

    printf( "Input the stop voltage: \n");  
    gets(ve);
    printf( "Input : %s\n",ve);

    printf( "Press any key to continue: ");  

    // ...and finally open the device driver
    printf( "Opening DAC: ");  
    dac = dac084s085_open( DRV_DAC084S085_1 );  
    puts( ( dac ? "OK" : "Fail" ) );
Appendix 11: View page of FPGA