Test Setup for LIN Transceiver TJA102x Family

FINAL REPORT
Test Setup for LIN Transceiver TJA102X Family

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Summary

The test setup for TJA102x family is used for failure testing LIN Transceiver which includes the chips named TJA1020, TJA1021, TJA1022, TJA1024, TJA1027, TJA1028, TJA1029 and UJA1018. Normally, the testing system contains six parts which is SMU (Source Measurement Unit), DAC (digital to analog converter), ADC (analog to digital converter), Oscilloscope, Power I/O and the test setup for TJA102x family. First five devices are used for power supply or data measurement which will have a basic description later. The test setup, the thesis project product, contains two parts: the hardware design and software design. The main functions of this product are explained as followed:

1. The automatic control:
   By the software program, a tester can control the external devices which is SMU, DAC, ADC, Oscilloscope and Power I/O automatically to send the voltage supply and some typical signal which can trigger certain function of the chip and read back the data through the test setup.

2. The accurate data transceiver
   The hardware of the test setup can accurately receive the signal from the external devices and send back the required data to those devices so that the tester can see the result of the test.

The main task of the test-setup will be introduced as followed:

1. The hardware design improvement:
   Previous design by Hieronimus Jonathan who had a trainee experience in NXP meets the basic needs of the measurement for TJA102x family: all the pins of the chips have been connected to the suitable devices in his schematic design. But the old design is not suitable for LIN transceiver TJA1024 anymore. How to add a 24 pins chip to the hardware design which is designed for 16 pins without causing the room problem of PCB and how to solve the pin compatible problem will be the uppermost topic of the thesis project. Changing the switch circuitry which includes the biggest space occupied relay will be the key point. Detailed research and test result for the new switch circuitries will be discussed deeply in the report.

2. The software program:
   Perfect hardware should be proved by a smart software program. The software program can have the basic control of the PCB board including checking whether all the switch circuits are working correctly, which is called as automatic board checker.
Foreword

This thesis is a part of the work required for the fulfillment of the Bachelor degree in Electrical Engineering in Hz University of Applied Sciences. What’s more, the thesis is important for people who will continue debugging the PCB board and design further. I would like to show my respect to my company mentors John van Zwam and Brecia Nurastu Sasongko. They not only taught me some practical knowledge about electrical design but also they gave me a lot of advice about the future career. Without their help, this project wouldn’t go that smoothly and successfully. I also wish to thank my school supervisory teacher Ad van Rijswijk. He guided me how to put the practical project into research level and also gave me lots of advice on the project. What’s more, I really appreciate the help from other colleagues during the internship. All in all, it is my honor to have the graduation internship in such a good company NXP Semiconductor Nijmegen.

The structure of the report shows below:

**Chapter 1: Introduction**
In this chapter, there is global background information of NXP Semiconductor and the test setup for LIN transceiver TJA102x chip family. Also, it shows the main question and sub questions of this project.

**Chapter 2: Theoretical Framework**
In this chapter, there tells the relevant knowledge with the project and describes the basic working theory of local interconnect networking (LIN) and LIN transceiver.

**Chapter 3: Design Methodology**
In this chapter, there shows the research methodology, structure development method (SDM), which was applied to the project.

**Chapter 4: Results**
In this chapter, there demonstrates the results of the project according to the method mentioned in chapter 3.

**Chapter 5: Conclusions**
In this chapter, the conclusion is made according to the results in chapter 4.

**Chapter 6: Recommendations**
In this chapter, several improvements for the future are mentioned.

**Appendix:**
Appendix shows the Hardware schematic design and software code.
Abbreviations

- ADC: Analog-to-Digital Converter
- BEV: Bird’s Eye View
- CAN(bus): Controller Area Network(Bus)
- DAC: Digital-to-Analog Converter
- EPD: End Product Definition
- ESD diode: Electrostatic Discharge diode
- GUI: Graphical User Interface
- IVN: In Vehicle Networking
- LIN: Local Interconnect Network
- NXP: NXP Semiconductor N.V.
- PC: Personal Computer
- SMU: Source Measurement Unit
- SDM: Structure Development Methodology
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1. Introduction

1.1 Background information

1.1.1 Background information of NXP Semiconductor
NXP Semiconductors is a semiconductor manufacturer. It is one of the worldwide top 20 semiconductor sales leaders and was founded in 1953, when the Philips Board started a semiconductor operation with manufacturing and development in Nijmegen, Netherlands. Formerly known as Philips Semiconductors, the company was sold by Philips to a consortium of private equity investors in 2006. The new name, NXP, stood for the consumer’s ”next experience”, according to then-CEO Frans van Houten.

NXP Semiconductors provides mixed signal and standard product solutions based on its RF, analog, power management, interface, security and digital processing expertise. More informally, NXP has characterized its strategy as focusing on "products with no big chip in the middle." These semiconductors are used in a wide range of "smart" automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing applications.

NXP is the co-inventor of near field communication (NFC) technology along with Sony and supplies NFC chip sets which enable mobile phones to be used to pay for goods, and store and exchange data securely.

In addition, NXP is the global market leader in many other areas, including automotive chips for in-vehicle networking, passive keyless entry and immobilization, and car radios, as well as silicon tuners for the TV and set-top-box market. As of February 2011, NXP had shipped over one billion ARM processor-based chips, and with its LPC microcontrollers, NXP is the only provider of microcontrollers with a roadmap based exclusively on 32-bit ARM architecture. NXP invented the I²C interface over 30 years ago and is the number one supplier of I²C solutions in the world. NXP is also the number one volume supplier of standard logic devices, and celebrated its 50 years in logic in March 2012. (1)
1.1.2 Background information of the TJA102x test setup

The local interconnect network (LIN) transceiver, TJA102X, are widely used in the field of automotive network. Although NXP has refined manufacturing equipment, still the company receives complains about the abnormal working condition of LIN transceivers. When we receive customer complain, complaining handling group consists of product engineer, designer and failure analyst engineer works together to find the root cause. To figure out the problem, Design support group has built test setups dedicated for different type of LIN transceivers.

At first, the design support group built several manual-check boards for TJA102x test setup. The figure shows the manual-check board for TJA1027. The tester just supplied the voltage to the pins and checked the value by multi-meters. But to measure the pins one by one is time consuming and a waste of human resources. It is necessary to develop a test setup which can be controlled by the software program. Figure 2 demonstrates the manual way of testing.

![Figure 2 Manual way of testing](image)

Then the design support group developed the board of digital-to-analog-converter (DAC), analog-to-digital-converter (ADC), power I/O, power supply board. These boards are connected to the personal computer (PC) through FTDI module USB/I²C board. Also, source measurement unit (SMU) is used as a voltage source to measure the current or as a current source to measure the voltage. Moreover, the group designed a motherboard as a data transfer station between the external measurement devices and the daughterboard. The daughterboard is the device used to transmit the signal from the chip and the external measurement devices.

The first version of TJA102x came out by Hieronimus Jonathan, a student from Fontys University of applied sciences. His design fulfills the basic test requirements for TJA1020, TJA1021, TJA1022, TJA1027, TJA1028, TJA1029 and UJA1018. Since the trainee time was short, he only made the schematic design for the daughterboard. His design includes 22 schematic design sheets which are for 16 pins test setup. (2)

---

1 The power supply board can supply 3V3, PVCC, +5V, -5V, +12V and -12V.
1.1.3 What is needed to be improved for the previous design?

Originally the project was to check the first version design and mainly focus on making the software program for that. However, new requirement arouse that TJA1024 should also be tested by the test setup. It is inevitable that some problems emerge.

A. Mechanical relay is too big

Since a new chip TJA1024 should be added in the test setup which will increase the number of the pins and also require some protection for the external devices especially DAC, Difficulty of improving the original hardware design version emerged: More than 150 components will be added into the PCB board including more than 20 DPDT D2n Relay V23105 which dimension is 20x10x11mm. As showed in figure 3, the PCB board is already crowded. To solve the problem, an idea has aroused: Can any smaller components replace the relay?

B. Design pin by pin is a waste of components

TJA1024 has 24 pins to the test setup. 8 more pins will be added which means 8 more schematic designs. It is estimated that there will be 150 components increase in the daughterboard. It’s impossible to make the design fit the PCB board as mentioned before. Also design pin by pin is a waste of components. The task is: How to design the circuit without adding new schematic sheets for new pins?

C. Problem of Pin incompatible

Fig 4 shows the pin map for the daughterboard. From the pin map we can see that chip TJA1020, TJA1021, TJA1022, TJA1024, TJA1027, TJA1029 are almost pin compatible. But chip TJA1028 and UJA1018 are not pin compatible to other chips. It is not easy to design for the pin which mixed the high power pin and the low power pin. Also, TJA1024 has a different footprint package. What can be done with the PIN incompatible chips?

2 The pin structure for TJA1024 is not line in two columns but 4 pins locate at the upper and bottom
1.2 Theme and goal of the thesis

The main theme of the thesis is to show the improvements of the test setup. The main question of the thesis is:

**How to improve and build the test setup for TJA102x family which can transmit the data from the external devices to the chips and the other way around?**

The sub questions of the thesis will be:

- **What is LIN?**
- **What is LIN Transceiver (TJA102X family)?**
This will be answered in chapter 2 theoretical framework.
- **What is needed to be improved for the previous design?**
This will be answered in chapter 4.1 problem analysis phase: a list of improvement.
- **What is the specification of the daughterboard?**
This will be answered in chapter 4.1 problem analysis phase: bird's eye view (BEV) and end product definition (EPD).
- **What is the functional block of the daughterboard?**
This will be answered in chapter 4.2 external problem definition and internal problem definition.
- **What kind of components can realize each functional block mentioned in internal problem definition phase?**
- **What is the specification of the functional circuit which is designed in functional design phase?**
This will be answered in chapter 4.3 Functional design and physical design of the daughterboard.
- **How to make a User-friendly graphical user interface (GUI)?**
- **What is the functional block of the program?**
- **What's the logic idea of the software?**
- **What kind of code can send data to the test setup?**
This will be answered in chapter 4.4 software design.
2. Theoretical Framework

2.1 Brief Overview of the relevant knowledge

Since the test setup design includes two parts, hardware design and software program design. The brief overview of knowledge will also be split into two parts, knowledge of hardware design and knowledge of software design.

For hardware design, on the one hand, it is important to acquire the knowledge of analog electronics. In this project, basic proficiency of applying relays, transistors, switches, diodes and capacitors are required. On the other hand, it is necessary to have a good command of Altium (shows in figure 5), the software used for designing. For software design, Borland Delphi 5 (shows in figure 6) is necessary.

Last but not least, the whole design should be on the basis of the knowledge of the operation of the TJA102x family. (TJA1020 (3), TJA1021 (4), TJA1022 (5), TJA1024, TJA1027 (6), TJA1028 (7), TJA1029 (8), UJA10018 (9)). Figure 7 shows the data sheet of LIN transceiver.

2.2 Local Interconnect Network

What is local interconnect network (LIN)?

LIN (Local Interconnect Network) is a kind of bus protocol which is designed for low-cost communication between smart sensors and actuators in automotive applications for example the air conditioning, seats, mirrors,
rain sensors, light sensors, door locking and windows and so on. The basic construction is displayed in figure 8. The speed of LIN is 20kb/s.

Lin bus has a lot of advantages. As Figure 9 shows that if no multiplexing is used and each device connects to the centralized body computer, then almost 113 wires are used for the connection. This architecture costs wires. Moreover if there are some changes like adding one more load to the system, much effort will be taken. Figure 11 shows the approach of utilizing CAN bus. With a little less number of wires, the problem of hard to change the system still exists. A clever method comes out with the application of LIN bus. As showed in figure 10, LIN bus line replaces large numbers of wires and makes the simplification of the system. A load can be added to a vehicle by plugging a Smart Connector to the bus and modifying the software in master. This makes the sub-system plug and play. Also the price of the LIN bus is twice cheaper than the CAN bus and flex ray. (10)

2.3 LIN transceiver TJA1020

What is LIN transceiver?

TJA1020 is NXP’s first LIN transceiver. Normally it transmits data for rain sensor, wiper motor, switch panel, steering wheel module and so on.

As shown in the figure 12, TJA1020 has 8 pins in total. They are RXD, NSLP, NWAKE, TXD, GND, LIN, BAT, and INH.

Figure 13 shows the common application of TJA1020. Normally LIN bus is connected to the LIN transceiver directly and
microcontroller is connected to the LIN transceiver. If there is a data signal from the LIN bus, the transceiver will receive the data from LIN pin and send it to the microcontroller via RXD. If there is a data signal from the microcontroller, the transceiver will receive the data via TXD pin and send it to the LIN bus. Usually the microcontroller is connected to the sensor or an actuator. INH pin is connected to the voltage regulator to give power supply for it. NWAKE pin is pulled up to the \( V_{BAT} \) and have the function of the local wake-up.

TJA1020 has four modes. Sleep mode, standby mode, normal slope mode and low slope mode. Sleep mode is the most power saving mode and the default mode after the power supply on battery pin. Standby mode is entered after the local or remote wake up occurs while TJA1020 is in sleep mode. There are two working mode for TJA1020, one is the normal slope mode and the other is low slope mode. In these two modes the chip can both receive and transmit data from the LIN bus line or micro controller. The difference between two modes is the bus signal transition time. The transition time of the low slope mode is about two times longer than that of the normal slope mode.

### 2.4 LIN transceiver TJA1028 and UJA1018

The testing chips TJA102x family can be classified into two groups according to their function. One is called stand-alone transceiver which includes TJA1020, TJA1021, TJA1022, TJA1024, TJA1027 and TJA1029. Another is called system basis chip (SBC) which includes TJA1028 and UJA1018. Based on the conventional function of the LIN transceiver as mentioned before, TJA1028 and UJA1018 have the voltage regulator inside which save the space of an electronic control unit (ECU). Moreover, TJA1028 and UJA1018 have RSTN pin which can reset microcontroller when the VCC is too low. Figure 14 and 15 depict the block diagram of TJA1028 and UJA1018.
3. Design Methodology

3.1 Introduction of SDM

Structured development method (SDM) will be applied to the project. Structure Design Methodology is commonly used to the systematic design like integrated circuit (IC) design. As what is showed in the picture that there are several processes. These processes are very useful to solve the problem. With problem analysis phase, Bird’s Eye View is a visual representation of the problem within its environment without much detail. Also it can be used as intermediary when talking to a costumer. End Product Definition (EPD) defines the usability of the system for the end-user. The main features are described in the EPD. There are 2 parts in the problem definition phase. One is external problem definition and another is internal problem definition. In the external problem definition, the interfaces of the design problems will be defined. The next step is to zoom in the problem and make an internal overview of the problem. Then it goes to the design part: functional design and physical design. In the functional design, we describes the system in terms of WHAT it does, not how and focused on the USABILITY, not operability. Jargon is not allowed in the functional design. In the physical design, we describes the system in terms of HOW, not what and focuses on OPERABILITY, not usability. JARGON language is allowed in the physical design. (11)

3.2 Justification

In problem analysis phase, bird’s eye view and end product definition would show a clear overview of the whole project and explain all the measurement tools used in the lab. Moreover, a list of improvements would also be included.

In External problem definition phase, an external overview defines the signal value and type which would transfer into the daughterboard. In internal problem definition phase, internal overview of the daughterboard gives a clear view of the structure. Each block in the internal overview diagram would be realized into a schematic design. There would be no contract part in this project.

The contents of functional design phase and physical design phase of hardware are mainly about the improvements in hardware design. For software, the functional design would describe how to make the automatic board checker and physical design would be the code in
Appendix.
In the realization phase, it would show the test board. A test board was made to check whether the new concept could work as expects and whether the software could send the command. Also, the testing result and analysis would be written there.
Since it takes time for manufacturing the daughterboard, there is not time for me to writing the testing result into the final report. But this part would be showed in the presentation.
4. Results

4.1 Problem analysis phase

4.1.1 A list of improvements
As mentioned before, there are 3 difficult questions should be answered when improving the hardware design: Can any smaller components replace the relay, how to design the circuit without adding new schematic sheets for new pins and what can be done with the PIN incompatible chips.

4.1.2 Birds eye view

Figure 17 represents bird’s eye view (BEV) of the whole testing system. It shows the relation between the daughterboard, the motherboard and other measurement devices which are SMU (source measurement unit), DAC/ADC (digital to analog converter/analog to digital converter) Power I/O and Oscilloscope. Power I/O is an open collector output which connects the circuit to the ground. SMU is to supply the voltage which is larger than 5V and measure the current of each pin. DAC is to supply the voltage which ranges from 0V to 5V. ADC is to measure the voltage which is larger than 5V and ranges from 0V to 5V. Oscilloscope is to measure the voltage waveform of each pin. Mother board is to transmit the data between all the external devices and the test setup just like a transfer station. Different types of transceiver’s daughterboard can be plugged into the same motherboard to do a chip testing task.

Tester uses the software which is programmed by Delphi5 to control the whole test setup. Suitable measurements tool (SMU/ADC/DAC/Oscilloscope/Powr I/O) will be triggered and send back the data to the software so that the testing result can be read easily and clearly by the tester on PC. The detailed information of the measurement tools are explained in appendix C.
4.1.3 End Problem Definition

This is the End Product Definition (EPD). Figure 18 shows a product which the company mentors required. The size of the PCB board is 170mm * 240mm. There will be several parts on the board. The first is the SMB bus connector which is used to connect to the oscilloscope. The second part is the connector to the motherboard. The third part is a thermal test circle. The area inside the circle will be heating up or cooling down when doing the temperature test. Inside the circle, the component like LED should not be there, otherwise the components will be broken when heating the board. Inside the circle there is a 24 pins socket which is used to connect the chip with the daughterboard. The pin probes nearby are used when some manual test is needed.

4.2 External Problem Definition

This is an external overview of the daughterboard (Figure 19). It explains the connection between daughterboard and other external devices. It is necessary to connect the measurement devices to the daughterboard. To make every connection selective, switch circuit controlling is very important. It decides which pin is connected to which measurement devices. NXP produces a lot of daughterboards for testing the customer complain chips. The motherboard is used as a platform for the daughterboard.
4.3 Internal Problem Definition for hardware

Figure 20 Internal Overview of the daughterboard

Figure 20 shows an internal Overview of the daughterboard. The test setup is made to measure the current and voltage for each pin. After studying the data sheet of all the chips, it is useful to classify the pins according to their power specification. One benefit is that the schematic design will be simple. The other one is that the components can be chosen more efficient. For example, if the low power pin only needs 10V voltage supply, then the switch circuitry contains 220VDC relay is not necessary.

According to the requirement made by the company mentors, circuitry which can trigger and measure the test mode of the chip should be considered into the daughterboard. Figure 21 shows the diagram of test mode. Detailed information about test mode is explained in the appendix A.

All the blocks discussed above will be connected to a chip module which called the top level connection. The top level connection makes the schematic methodical. Otherwise the whole design will be in one schematic and makes the design looks like a spider and even more mistakes will be made.

Finally the top connection will be the bridge for the motherboard connector and daughterboard connector.
4.4 Functional Design and Physical Design of the improvement of hardware

4.4.1 Can any components replace the mechanical relay?
In the schematic design of LIN termination (Figure 22), relays are used as switches to control which external devices should be connected to which pins. Detailed information about the three relays are demonstrated in Jonathan’s report (2).

To find suitable circuit to replace the relay, it is necessary to define the specification for the circuits. According to the requirements from data sheet, the substitutes should handle 60V. After investigations, there are two solutions to replace the relay.

**Solution 1: Transistor Switch**

In the application of switches, P-MOS and N-MOS combination is often used to the circuit. Figure 23 demonstrates one of the common applications.

A resistor in parallel with the P-MOS and N-MOS has two functions. One is for discharging the P-MOS gate capacitor, another one is to make the voltage at position A as the same as the voltage at position B when N-MOS is not conducted.

An N-MOS is used to control the gate voltage of P-MOS. If a low voltage is supplied to the gate of N-MOS, N-MOS is not conducted. Va = Vb, P-MOS is not conducted neither, the pin can’t get the input voltage supply. This situation is called switching off. If a high voltage is supplied to the gate of
N-MOS, N-MOS is conducted, \( V_a = 0 \) which means a low voltage is supplied to the gate of P-MOS, P-MOS is conducted, Pin voltage will be equal to the voltage input.

In the physical design (Figure 25), some protection for the circuit is necessary. First is the zener diode. According to the characteristics of zener diode (BZT52H-C5V6), voltage across the zener diode will be clamped between 5.2 and 6.0. If there is no voltage controlling for the P-MOS transistor, \( V_{gs} \) can be higher than 20V which will damage the gate of power FET.

The second protection is the pull-down resistor. The pull down resistor is used to protect the pin if the pin doesn’t have the pull down construction inside. The resistor is necessary because when the MOSFET is not conducted, the drain side will become high \( \Omega \). Because of the leakage current from the source side, then the pin voltage will be as high as the supplied voltage which would damage the pin itself.

With the simulation, the transistor switch is proved to have the same function as a relay. The following picture shows the simulation result. (X-axis is time; Y-axis is Voltage) .12V pulse voltage is assumed as voltage supply.
Condition 1:
V1 is supplied pulse voltage, V2 is 5V, V3 is 5V, V4 is 0V, and the simulation result is as followed.

Condition 2:
V1 is supplied pulse voltage, V2 is 5V, V3 is 0V, V4 is 5V, and the simulation result is as followed.

Condition 3: V1 is supplied pulse voltage, V2 is 0V, V3 is 0V, V4 is 0V, and the simulation result is as followed.

Conclusion: As explained in figure 17, 1 transistor switch still needs 6 components. The advantage of reducing the components is not obvious compared with the switch circuitry with mechanical relay. The cost of one transistor switch is: €0.39 (BSH201) + 0.062 (zener diode) + €0.31 (2N7002) + €0.2 (two 10k resistor) = €0.962. It is much cheaper than the construction of mechanical relay. The solution is considerable.
**Solution 2: Solid State relay, Optocoupler**

In electronics, an optocoupler is a component that transfers electrical signals between two isolated circuits by using light. Figure 26 to Figure 29 show the construction of the solid state relays. It prevents high voltages from affecting the system receiving the signal. A common type of optocoupler consists of an LED and a phototransistor in the same opaque package. (12)

To fit the requirement, Assr1218 and Assr1228 will be used. According to the data sheet, the range of Vout is from -60V to +60V, the average output current is up to 0.2A and the output power dissipation is up to 400mW. One of its applications is reed relay replacement.

According to the description from the data sheet, the relay turns on (contact closes) with a minimum input current of 3 mA through the input LED. The relay turns off (contact opens) with an input voltage of 0.8V or less. Since there is no Assr1218 in the lab, the following experiment will be done with Assr1228.
Functional design for the test circuit

Physical Design of the test circuit

R1 = R2 = 330 Ω; R3 = R4 = 1K

The type of the red LED is 597-3021-5xx, the forward current is up to 25mA, the forward voltage is 2V. The input forward current of the optocoupler is from 3mA to 20mA, normally, 5mA is chosen for the testing condition. A resistor is chosen to limit the current.

\[ R_{1,2} = \frac{V_d-V_{LED}-V_{assr1228}}{I_F} = \frac{5V-2V-1.3V}{0.005A} = 340\Omega \]

Table 1 Dual switch function test.

<table>
<thead>
<tr>
<th>1. Initial condition</th>
<th>2. both Switch on</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vd1= 0V, Vd2 = 0V; (Diode side switch)</td>
<td>Vd1 = 5V , Vd2 = 5V; (Diode side switch)</td>
</tr>
<tr>
<td>Vs1 = 0V, Vs2= 0V ; (switch side switch)</td>
<td>Vs1 = 5V, Vs2 = 5V ; (switch side switch)</td>
</tr>
</tbody>
</table>

3 Red LED on

4. Green LED on

Vd1 = 5V , Vd2 = 0V; (Diode side switch); Vs1 = 5V , Vs2 = 5V ;(switch side switch)

Vd1= 0V, Vd2 = 5V; (Diode side switch); Vs1 = 5V, Vs2 = 5V ;(switch side switch)
Conclusion:
This is a function test of the optocoupler. This test proves that assr1228 and ass1218 meet the needs of the function of a dual channel switch. As written in the data sheet that the typical value of output leakage current is 0.005uA which means that high voltage (60 V) applied on the switch when the switch is off, nearly no current goes through the switch. It will be wise to use it to replace the relays.

Solution3: Analog Switch
There are 3 schematics made by Jonathan. They are CLK line, Voltage controller and data line. Figure 30 shows the specification for test mode.

![Figure 30 Test mode specification](image)

As all the voltage level is not high, it’s not necessary to use the COTO TECHNOLOGY – 9012 which can stand 200V according to the data sheet. (13) For this situation which the clock(CLK) signal and data signal are not higher than 5V, analog switch comes up with its small size and low price. In the lab, there is a type of analog switch called ISL43112. Figure 31 shows the internal structure of ISL43112.

![Figure 31 ISL43112 Diagram](image)

4.4.2 How to design the circuit without adding new schematic sheets for new pins?
After one and half month working in NXP, a new task is announced by the company mentors: the daughterboard should be also applied to testing chip TJA1024. As it is said before, it is impossible to add 8 more schematics for 8 more pins. A clever way should be discovered.

Since the structure of TJA1024 is not compatible with the socket for other chips. So the adapt board will be made to make the pin for TJA1024 locate in two columns just like other chips do. Figure 32 shows the adapted image of the TJA1024.

![Figure 32 TJA1024 adapted image](image)

3 The pin structure for TJA1024 is not line in two columns but 4 pins locate at the upper and bottom side of the chip.
Compare the internal structure between TJA1022 and adapted TJA1024, it is not hard to find that adapted TJA1024 is actually double TJA1022 with some small differences. Moreover, the left side of adapted TJA1024 can be separated as 2 parts: upper part and lower part. Then an idea came into mind: shifting pins by the switch!

The physical design for pin shifting is showed in fig 33. Optocoupler assr1228 is used in this design as a dual switch. The electronic trick used in this design is in the LED side. To increase the convenience for software programming, only one DAC port is put to control the switch. If PINa-b gives 0V supply, Pina will be connected to the main circuit. If PINa-b gives 5V supply, Pinb will be connected to the main circuit.

**4.4.3 What can be done with the PIN incompatible chips?**

As mentioned before, one difficulty of the improvement is pin incompatible.

---

4 It connects to the DAC (Digital to Analog Converter)
Let’s zoom into Pin1 (Figure 34). In pin1, there are 2 kinds of pins: RXD (Low power pin) and VBAT (High power pin). For assr1218 and assr1228, the maximum current is 200mA and the voltage is 60V. As showed in the data sheet of TJA1024 the voltage range of RXD pin is around -0.3V to 7V and current is around 2mA. In the data sheet of TJA1028, The voltage range of VBAT is 5.5V to 28V and the sink current is possibly come up to 250mA. The conclusion is that the Optocoupler cannot be used in pin1 according to the battery pin. The same situation also happened in pin4 and pin21. So making an adapt board for TJA1028 and TJA1018 is necessary.

As told by the designer of TJA1028, UJA1018 is a derivative product from TJA1028. So the basic structure is the same. One adapted board will be made for two chips. Figure 35 shows the arrangement of all chips.

![Figure 35 Final pin map](image)

4.4.4 The protection for the DAC

From the data sheet, it is said that INH is an output pin which means the data will be transferred into the external device. Although the voltage range of INH is not that high from \(-0.3V\) to \((Vbat+0.3)V\), DAC can only handle the voltage range from 0 to 5V. Some protection should be considered to assure the DAC won’t be damaged with the exceeding value of the voltage from INH when the switch is happened to be closed. Figure 37 shows the functional design of the DAC protection.

According to the characteristics of the zener diode (Figure 36), the reversed voltage will be stable up to Vz when the reversed current increases to infinite.

![Figure 36 Characteristics of Zenor diode](image)

5 Vbat: -0.3V to 40V
A zener diode is put in parallel with the DAC so that the voltage drop through the DAC will be clamped by the zener diode. A resistor is put there to limit the current which goes through the zener diode. Physical Design for the protection (Figure 38): The type of zener diode is NXP - BZT52H-C5V1. As showed in the data sheet that the voltage will be clamped to 5.6V. Under the protection of the zener diode, DAC won’t be damaged even if the switch is closed improperly.

4.5 Functional Design and Physical Design of the software

4.5.1 Software function definition:
The function of the software is to check whether the switches which connect to DAC, ADC, SMU, VCC can normally work or not. It is called: Automatic board checker. When the user starts the test setup, he has to calibrate the board first. He starts the automatic board checker, press the start button, the board will check those switches from pin 1 to pin16.

4.5.2 How the software works?
In the low power pin schematic, there are four switches need to be check. For example, DAC sends 5V. ADC measures the 5V. If the data can be transmitted correctly, then the switches are in a good working condition. The difficulty is 4 switches will have 16 ways of comparing. According to the characteristics of the schematic design, an idea came up. As VCC connects to the pull up resistor, there must be current when switch of VCC is turned on. Then, the solution comes up for four switches situation.

4.5.3 Solution for 4 switches
There are 2 steps for checking the switches. Firstly, the switches of VCC, SMU and ADC were turned on. SMU was set to 3V and measure back the current. ADC was used to measure the 3V. The detailed measurement process can be checked in the following table.

<table>
<thead>
<tr>
<th>No.</th>
<th>VCC</th>
<th>SMU voltage/current measured</th>
<th>ADC</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5V</td>
<td>3V</td>
<td>YES</td>
<td>3V</td>
</tr>
<tr>
<td>2</td>
<td>5V</td>
<td>3V</td>
<td>NO</td>
<td>3V</td>
</tr>
<tr>
<td>3</td>
<td>5V</td>
<td>3V</td>
<td>NO</td>
<td>5V</td>
</tr>
<tr>
<td>4</td>
<td>5V</td>
<td>3V</td>
<td>YES</td>
<td>0V</td>
</tr>
<tr>
<td>5</td>
<td>5V</td>
<td>3V</td>
<td>NO</td>
<td>0V</td>
</tr>
</tbody>
</table>

Table 2 First step check

After first step checking, there comes the second step checking. According to the result in first step checking, for example in case 1-3 ADC works normally, then ADC was used to do the second step check with DAC. In case 4, ADC works abnormally, then SMU was used to do the
second step check with DAC. Detailed process was explained in table2.

<table>
<thead>
<tr>
<th>No.</th>
<th>DAC</th>
<th>ADC</th>
<th>SMU</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5V</td>
<td>5V</td>
<td></td>
<td>All switches works perfectly</td>
</tr>
<tr>
<td></td>
<td>5V</td>
<td>0V</td>
<td></td>
<td>DAC switch has problem</td>
</tr>
<tr>
<td>2</td>
<td>5V</td>
<td>5V</td>
<td></td>
<td>VCC switch has problem</td>
</tr>
<tr>
<td></td>
<td>5V</td>
<td>0V</td>
<td></td>
<td>VCC switch and DAC switch have problems</td>
</tr>
<tr>
<td>3</td>
<td>5V</td>
<td>5V</td>
<td></td>
<td>SMU switch has problem</td>
</tr>
<tr>
<td></td>
<td>5V</td>
<td>0V</td>
<td></td>
<td>SMU switch and DAC switch have problems</td>
</tr>
<tr>
<td>4</td>
<td>5V</td>
<td></td>
<td>5V</td>
<td>ADC switch has problem</td>
</tr>
<tr>
<td></td>
<td>5V</td>
<td></td>
<td>0V</td>
<td>ADC switch and DAC switch have problems</td>
</tr>
</tbody>
</table>

Table 3 Second Step Check

4.5.4 Graphical User Interface

When opened the software, this is the first form. There is a main menu in the index form (Figure 39) which includes Calibration, LIN Transceiver and help. Beneath the menu of calibration, there is Automatic board checker (Figure 41). As showed in figure 40, when the relay is correct, it will show the correct image. If the relay is not working, it shows the cross image.
4.6 Realization

4.6.1 Test board

In the realization phase, a test board was made to check whether the analog switch and optocoupler can work properly or not. It has the same configuration as the real daughterboard. Figure 42 describes the schematic design of the test board and figure 43 shows the real test board.

![Test board schematic design](image)

**Basic structure information:**

Part 1 is a mechanical switch. In the real daughterboard design, this part was connected to DAC and received the logic low (input voltage less than 1.5 V) or logic high signal from DAC.

Part 2 is an analog switch ISL43112. -5V and +5V were respectively connected to V- (pin3) and V+ (pin5).

Part 3 is an optocoupler assr1228. It is used to be the switch for SMU.

Part 4 is a pin select switch as mentioned in page 18.
Test Result:
Figure 34 shows the test board. The upper part is analog switch and the lower part is optocoupler and pin select switch.
After testing, 2 problems showed up.

- Problem 1: The analog switch worked improperly.
  Phenomenon: As explained in the data sheet, ISL43112 is a normal open switch. So if logic high (5V) supply was given, the switch should be on and it can measure the voltage sent by SMU. But in practice, no voltage could be detected even from the pin1 and pin2 of the analog switch. But when the logic low (0V) supply was given, the voltage could be detected. Is there some shorts in the circuit?
  Action and Result: After checking the schematic design and the PCB layout, nothing strange in the design itself. So there must be some specification mistakes with the analog switch which is not noticed before. Then, ISL43113 came up. It is a normal close switch. Logic high input would make it open and logic low input would make the switch on. If the switch was ISL43113 instead of ISL43112, everything made sense. Finally it turned out that the supply number in the Altium library is not correct. So, the analog switch on the board was not ISL43112, but ISL43113.
  Improvement: All the analog switches in the daughterboard were checked and the supply number was changed to ISL43112.

- Problem 2: The P-MOS transistor worked improperly.
  Phenomenon: As mentioned in page 18, pin select switch circuitry which was constructed by 2 MOSFET transistors was an important application made for TJA1024. When there was logic low input, the P-MOS was conducted and LED D4 should be lighting up. But in practice, no matter logic high or logic low, the P-MOS never be conducted. The idea of the circuitry was wrong?
  Action and Result: First step, checking the schematic design and short circuit problem. As checked by the company mentors and other experienced colleagues, the idea of the circuitry was right. Second step, checking the data sheet of BSH201 (14) and footprint. The Altium library went wrong again. In the data sheet, pin1 is gate and pin3 is drain. But in Altium library, pin 1 and pin3 were swapped. Figure 44 shows the correct pin map of BSH201.

**PINNING**

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>gate</td>
</tr>
<tr>
<td>2</td>
<td>source</td>
</tr>
<tr>
<td>3</td>
<td>drain</td>
</tr>
</tbody>
</table>

**SOT23**

![Figure 44 BSH201 P-MOS PIN map](image)

Improvement: After changing the position of the BSH201, the pin select circuitry worked as expected. Also, the footprint in Altium was changed into the correct one.
4.6.2 Debugging the software on the test board

Before debugging the real daughterboard, firstly the software was tested on the test board. Since the analog switch are ISL43113 (normal close switch), the logic input (Part 1) was connected to the ground. Pin1 of ISL43113 was connected to the DAC. The input switch of SMU was connected to the Power I/O port. Figure 45 explains the connection of the circuit.

The goal: Check whether the software could properly send the command to the external devices.

The result: Figure 46 shows the correct result. The software worked as expected.

![Figure 45 Part schematic of the test board](image)

![Figure 46 One pin debugging](image)

4.6.3 The daughterboard

Figure 47 and figure48 shows the 3D model of the daughterboard.

![Figure 47 Front side of 3D model by Altium](image)
After 3 weeks manufacturing, the daughterboard will come around 28th of May. Below is the picture coming from the factory.
5. Conclusion:

The project was to improve and build a test setup for LIN transceiver TJA102x family which can transmit the data from the external devices to the chips and the other way around.

First of all, some study of LIN and LIN transceiver were made to get to know the project well. LIN was a low costing, one master chip multiple slave chips local interconnect networking system. It is widely used in automotive controlling system. LIN transceiver TJA102x family includes TJA1020, TJA1021, TJA1022, TJA1024, TJA1027, TJA1029, TJA1028 and UJA1018. First 6 chips are stand-alone chips and last 2 are system-basis chips. The difference between them is that SBC chips have a voltage regulator inside and it has RSTN pin to reset the microcontroller when the VCC supply becomes too low.

The project was to design a test setup for LIN transceiver, there should be a platform for the chips and it was the hardware part of the project, the daughterboard. The previous student Jonathan has already made a design for the daughterboard. As to improve the design, it was necessary to make the list of the improvements. 4 improvements were made according to the problem found, they were: mechanical relay was too big, Design pin by pin was a waste of components, problem of Pin incompatible and small protection was needed.

Since a new chip TJA1024 was added to the project, the size of the PCB was the critical problem needed to be solved in hardware design. After studying the switch circuitry, we found that there were three ways to replace the mechanical relays. They were the combination of N-MOS and P-MOS, solid state relay (optocoupler) and analog switch. To prove their reliability and practicability, a test board was made. From the experiment on test board, 2 severe components problems were found: 1. the supply number of the analog switch ISL43112 was not correct. 2. The footprint of P-MOS transistor in the Altium Lib was not correct. If these two problems couldn’t be solved, it would directly lead to a failure project. After analyze the experiment result, optocoupler, assr1218 and assr1228 were chosen to replace all the mechanical relays which were not only big but also expensive. Also, the clock line schematic and data line schematic design which had low voltage level characteristics used analog switch ISL43112.

Also, TJA1024 has 24 pins. Because of the special footprint of TJA1024, the adapted board has to be made for it to make it fit 2 columns socket. Previous design was made for maximum 16 pins chip. The PCB size was already small, 8 more schematics design pins would be critical and cost components. After checking the data sheet, the structure of TJA1024 has a mirror structure between upper part and lower part. Making a switch to shift between upper part and lower part became a solution.

Moreover, the daughterboard schematic design should be suitable for all the chips. But according to the original pin map, one pin schematic design combined not only high power
but also low power pin. It was difficult to choose suitable components for the mixed situation. Since TJA1020, TJA1021, TJA1022, TJA1024, TJA1027 and TJA1029 had almost the same structure, adapted boards were made for TJA1028 and UAJ1018. During designing the new pin map for the chips, the designer of TJA1028 advised me that only one board was enough for these 2 chips because UJA1018 is derived from TJA1028. This advice directly saved cost of one adapted board.

Last but not least, supporting software was necessary. In the project, an automatic board checker was made to calibrate the switch circuitry for VCC, DAC, ADC and SMU. The automatic board checker assures the reliability of the daughterboard. Although the real daughterboard couldn’t arrive on time, the testing on the test board proves the success of the software.
6. Recommendation:

In this project, several approaches for switch circuitry were investigated to replace the mechanical relay which could save PCB space and improve the reliability of the daughterboard. In the near future, current test boards will be redesigned using the concepts mentioned in this report. Moreover, the innovative application of the circuitry increases the feasibility of designing. Designing by power domain can be realized to replace conventional way of designing.

Because of the tight schedule, the software can only realize one function: automatic board checker. There are still more functionalities need to be implemented such as curve tracer measurement. Curve tracer measurement is to verify connection between board and integrated circuit (IC), which guarantees the validity of test result. Furthermore, test program for complete specification validation should be built.
6. Bibliography

3. PHILIPS. TJA1020 LIN transceiver. s.l.: PHILIPS, 2005.
14. NXP Semiconductor. P-channel enhancement mode BSH201.
Appendices

A. The schematic design of the daughterboard.

A.1 Low power pin schematic design

This is the low power pin schematic design. The schematic design was used for pin1 to pin6, pin10 to pin12. The current of the pin should be lower than 200mA, the voltage of the pin should be lower than 60V.

In part 1, ASSR 1218 was used for the connection to +5V (VCC), digital to analog converter (DAC), analog to digital converter (ADC) and oscilloscope. The type of LED is DIALIGHT - 597-3021-507F - LED, 1208, RED. Its forward voltage is 2V. To make the current 5mA, 340Ω resistor were chosen.

\[
R = \frac{V_{PVCC} - V_{LED} - V_{optocoupler}}{0.005A} = 340\Omega.
\]

In part 2, ASSR1228 was used as a DPDT mechanical relay. LED type was the same as part1.

\[
R = \frac{V_{12} - V_{LED} - 2*V_{optocoupler}}{0.005A} = 1000\Omega
\]

In part 3, transistor switch were used to shift between pin a and pin b. Also optocoupler ASSR1228 was used.
A.2 One pin schematic design

If it was not necessary for pin shifting, then we cut that part and saved components just like pin7, pin8, pin9 and pin14. The basic structure including SMU, DAC, ADC, and Oscilloscope was kept from the low power pin schematic.
Why there is a mixed application of solid state relay optocoupler and mechanical relay?
This is the schematic design for high power pin 15. For TJA1028 and UJA1018, the current from SMU1 (BAT pin supply) was higher than 200mA which was larger than ASSR1228 could handle. That’s why the DPDT mechanical relay was necessary. It could handle maximum 3A current.
The same as pin 15, this pin includes INH and VCC. Because of VCC, the current will go high up to 250mA. So mechanical relay was necessary, the capacitor was to eliminate the EME problem.
This schematic design is for LIN characteristic testing. The transceiver could play 2 roles in the network, master chip or slave chip. When the customer returns the failure chip, he would mention the role of the chip. If the master chip went wrong, then we connected the LIN Pin with 1k. If the slave chip went wrong, then the customer would mention the load whether it was 500Ω or 650Ω.
A.6 Test Mode—Data line
A.7 Test mode--Clock line (CLK)

CLK Line (DAC)
Typical RXD clock signal input
A.8 Test mode—Voltage controller
Test mode explanation:

After receiving the complain products from the customers, some special specifications would be tested such as the frequency of the oscillator inside the IC. To get the special specifications, it is necessary to enter the test mode of the chip.

This is the precondition to enter the test mode. NSLP pin would be supplied by the negative voltage. So we created voltage controller schematic. Data line was created to send the typical TXD value to the pin. CLK line was made to send the clock signal to RXD pin. For instance, supposed that test mode is essential to measure the frequency of the oscillator. According to the required signal, test mode was entered. Then, the switch of RXD would be connected to the oscillator instead of the receiver. In that case, we can measure the specification from the oscillator. All in all, test mode is needed for testing some special value inside the ICs.
A.9 Top connected
A .10 Top level connected
B Software physical design

B.1 Automatic Board Checker

unit bdchecker;
interface
uses
  Windows, Messages, SysUtils, Classes,
  Graphics, Controls, Forms, Dialogs,
  DAC, ADC1, ADCMT6240A1, PowerIO1,
  ExtCtrls, StdCtrls, hardwareform;
type
  TBdCheckerFORM = class(TForm)
    GroupBox1: TGroupBox;
    Label1: TLabel;
    Image1: TImage;
    Image2: TImage;
    Label2: TLabel;
    Image3: TImage;
    Image4: TImage;
    Image5: TImage;
    Image6: TImage;
    Label3: TLabel;
    Image7: TImage;
    Image8: TImage;
    Label4: TLabel;
    GroupBox2: TGroupBox;
    Label5: TLabel;
    Image9: TImage;
    Image10: TImage;
    Label6: TLabel;
    Image11: TImage;
    Image12: TImage;
    Image13: TImage;
    Image14: TImage;
    Label7: TLabel;
    GroupBox3: TGroupBox;
    Label8: TLabel;
    GroupBox4: TGroupBox;
    Label9: TLabel;
    GroupBox5: TGroupBox;
    Label10: TLabel;
    Image17: TImage;
    Image18: TImage;
    Label11: TLabel;
    Image19: TImage;
    Image20: TImage;
    Label12: TLabel;
    Image21: TImage;
    Image22: TImage;
    Label13: TLabel;
    Image23: TImage;
    Image24: TImage;
    Label14: TLabel;
    Image25: TImage;
    Image26: TImage;
    Label15: TLabel;
    Image27: TImage;
    Image28: TImage;
    Label16: TLabel;
    Image29: TImage;
    Image30: TImage;
    Label17: TLabel;
    Image31: TImage;
    Image32: TImage;
    Label18: TLabel;
    Image33: TImage;
    Image34: TImage;
    Label19: TLabel;
    Image35: TImage;
    Image36: TImage;
    Label20: TLabel;
    Image37: TImage;
    Image38: TImage;
    Label21: TLabel;
    Image39: TImage;
    Image40: TImage;
    Label22: TLabel;
    Image41: TImage;
    Image42: TImage;
    Label23: TLabel;
    Image43: TImage;
    Image44: TImage;
  end;
procedure FirstCheckOn(SMUtype: integer; SMUaddress: integer; SMUon: integer; ADCOn: integer; VCCon: integer);

This procedure is to turn on the relays of VCC, SMU, DAC and ADC

procedure FirstCheckOff(SMUtype: integer; SMUaddress: integer; SMUon: integer; ADCOn: integer; VCCon: integer);

This procedure is to turn off the relays of VCC, SMU, DAC and ADC

procedure FirstComeOut(SMUtype: integer; SMUaddress: integer; SMUon: integer; ADCOn: integer; VCCon: integer; DACout: integer; VCCimage1, DACimage1, ADCimage1, VCCimage2, DACimage2, ADCimage2, SMUimage1, SMU2image1, SMUimage2, SMU2image2: integer);

This procedure is to show the result of the 4 relay's check.

procedure SecondCheck1On(DACout: integer; DACon: integer; ADCon: integer);

This procedure is for second check to turn on the relays of DAC and ADC

procedure SecondCheck1Off(DACout: integer; DACon: integer; ADCon: integer);

This procedure is for second check to turn off the relays of DAC and ADC

procedure SecondCheck2On(DACout: integer; DACon: integer; SMUon: integer);
This procedure is for second check to turn on the relay DAC and SMU.

procedure
SecondCheck2Off(DACout:integer;DACon:integer;SMUon:integer);

This procedure is for second check to turn off the relay DAC and SMU.

function
FirstCheckResult(mvoltage,mcurrent:real):integer;
This function is for sending back the first comparing result (1-5) of first check.

function
SecondCheckResult(mvoltage2:real):integer;
This function is for sending back the second comparing result of first check.

procedure
Resultshow(Firstresult:integer;SecondResult:Integer;VCCimage1,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2:integer);
This procedure is for activating the image result.

procedure
result(VCCimage:integer;DACimage:integer;ADCimage:integer;SMUimage:integer;SMU2image:integer);
This procedure is for activating the image result.

procedure
imagenos(n:Timage);
This procedure is for making the image disappear. This procedure will be program for the stop button.

procedure imageno(p:Timage);
This procedure is for making the image item into number.

procedure imageshows(q:integer);
This procedure is for making the image appear.

procedure imageNshows(m:integer);
This procedure is for making the image disappear. This procedure will be program for the stop button.

procedure
OnePinSecondCheckon2(DACon,SMUon:integer);
This procedure is for the 3 relays checking situation. Turn on the relay of DAC and SMU.

procedure
OnePinSecondCheckon1(DACon,ADCon:integer);
This procedure is for the 3 relays checking situation. Turn on the relay of DAC and ADC.

procedure
NoVCCcheck(SMUtype,SMUaddress,ADCin,DACout,DACon,SMUon,ADCon,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2:integer);
This procedure is for the 3 relays checking situation.
situation without VCC. It shows the result of 3 relays check.

implementation

uses T1020;

{$R *.DFM}

procedure OnePinSecondCheckon1(DACon,ADCon:integer);
begin
bdcheckerFORM.PowerIO11.output_on(DACon);
bddcheckerFORM.PowerIO11.output_on(ADCon);
end;

procedure OnePinSecondCheckon2(DACon,SMUon:integer);
begin
bdcheckerFORM.PowerIO11.output_on(DACon);
bddcheckerFORM.PowerIO11.output_on(SMUon);
end;

procedure NoVCCcheck(SMUtype,SMUaddress,ADCin,DACout,DACon,SMUon,ADCon,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2:integer);
var
mvoltage:real;
mvoltage2:real;
begin
setSMUvoltage(SMUtype,SMUaddress,3,10e-4);
mvoltage:=TJA1020P.ADC11.ADCvalue(ADCin);
if (mvoltage>2.7) and (mvoltage<3.3) then 
begin
FirstCheckOff(SMUtype,SMUaddress,SMUon,ADCon,0);
sleep(500);
OnePinSecondCheckon1(DACon,ADCon);
bddcheckerFORM.DAC1.SendVolt(DACout,5);
//set 5V from DAC
mvoltage2:=TJA1020P.ADC11.ADCvalue(ADCin);
if (mvoltage2>4.7) and (mvoltage2<5.3) then 
begin
Resultshow(1,1,0,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);
SecondCheck1Off(DACout,DACon,ADCon);
end 
else 
begin
Resultshow(1,2,0,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);
SecondCheck1Off(DACout,DACon,ADCon);
end 
end
else if (mvoltage<0.5) and (mvoltage>=0) then 
begin
FirstCheckOff(SMUtype,SMUaddress,SMUon,ADCon,0);
sleep(500);
OnePinSecondCheckon1(DACon,ADCon);

bdcheckerFORM.DAC1.SendVolt(DACout,5);
//set 5V from DAC

mvoltage2:=TJA1020P.ADC11.ADCvalue(ADCin);
if(mvoltage2>4.7) and (mvoltage2<5.3) then

begin

Resultshow(3,1,0,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);

bdcheckerFORM.PowerIO11.output_off(ADCon);

end

else

begin

bdcheckerFORM.PowerIO11.output_on(SMUon);
mvoltage2:=measureSMUvoltage(SMUtype,SMUaddress);

if(mvoltage2>4.7) and (mvoltage2<5.3) then

begin

Resultshow(5,1,0,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);

bdcheckerFORM.PowerIO11.output_off(SMUon);

end

end

end;

procedure FirstCheckOn(SMUtype:integer;SMUaddress:integer;SMUon:integer;ADCon:integer;VCCon:integer);

begin

hardwareform.setSMUvoltage(SMUtype,SMUaddress,0,10e-3);//SMUclear

bdcheckerFORM.PowerIO11.output_on(SMUon);//close SMUon relay

bdcheckerFORM.PowerIO11.output_on(ADCon);//close ADCon relay

bdcheckerFORM.PowerIO11.output_on(VCCon);//close VCCon relay

hardwareform.setSMUvoltage(SMUtype,SMUaddress,3,10e-3);//SMU set 3V

end;

procedure FirstCheckOff(SMUtype:integer;SMUaddress:integer;SMUon:integer;ADCon:integer;VCCon:integer);

begin

end
begin

setSMUvoltage(SMUtype,SMUaddress,0,10e-3);//SMUclear

bdcheckerFORM.PowerIO11.output_off(SMUon);//open SMUon relay

bdcheckerFORM.PowerIO11.output_off(ADCon);//open ADCon relay

bdcheckerFORM.PowerIO11.output_off(VCCon);//open VCCon relay
end;

procedure FirstComeOut(SMUtype:integer;SMUaddress:integer;SMUon:integer;ADCon:integer;VCCon:integer;DACon:integer;ADCin:integer;DACout:integer;VCCimage1,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2:integer);
var
mvoltage,mcurrent,mvoltage2:real;
e,f:integer;
begin

mvoltage:=TJA1020P.ADC11.ADCvalue(ADCin);
mcurrent:=measureSMUcurrent(SMUtype,SMUaddress);

e:=FirstCheckResult(mvoltage,mcurrent);
case e of
1,2,3: begin
FirstCheckOff(SMUtype,SMUaddress,SMUon,ADCon,VCCon);
sleep(1000);
SecondCheck1On(DACout,DACon,ADCon);
mvoltage2:=TJA1020P.ADC11.ADCvalue(ADCin);
f:=SecondCheckResult(mvoltage2);
Resultshow(e,f,VCCimage1,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);
SecondCheck1Off(DACout,DACon,ADCon);
end;
4: begin
FirstCheckOff(SMUtype,SMUaddress,SMUon,ADCon,VCCon);
sleep(500);
SecondCheck2On(DACout,DACon,SMUon);
mvoltage2:=measureSMUvoltage(SMUtype,SMUaddress);
f:=SecondCheckResult(mvoltage2);
Resultshow(e,f,VCCimage1,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);
SecondCheck1Off(DACout,DACon,SMUon);
end;
5: begin
FirstCheckOff(SMUtype,SMUaddress,SMUon,ADCon,VCCon);
result(VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);
end;
end
end;

procedure
SecondCheck1On(DACout:integer;DACon:integer;ADCon:integer);
begin
bdcheckerFORM.PowerIO11.output_on(DACon);//close DACon relay
bdcheckerFORM.PowerIO11.output_on(ADCon);//close ADCon relay
bdcheckerFORM.DAC1.SendVolt(DACout,5); //set 5V from DAC
end;

procedure
SecondCheck1Off(DACout:integer;DACon:integer;ADCon:integer);
begin
bdcheckerFORM.DAC1.SendVolt(DACout,0); //set 0V from DAC
bdcheckerFORM.PowerIO11.output_off(DACon);//open DACon relay
bdcheckerFORM.PowerIO11.output_off(ADCon);//open ADCon relay
end;

procedure
SecondCheck2On(DACout:integer;DACon:integer;SMUon:integer);
begin
bdcheckerFORM.PowerIO11.output_on(DACon);//close DACon relay
bdcheckerFORM.PowerIO11.output_on(SMUon);//close SMUon relay
bdcheckerFORM.DAC1.SendVolt(DACout,5); //set 5V from DAC
end;

procedure
SecondCheck2Off(DACout:integer;DACon:integer;SMUon:integer);
begin
bdcheckerFORM.DAC1.SendVolt(DACout,0); //set 0V from DAC
bdcheckerFORM.PowerIO11.output_off(DACon);//open DACon relay
bdcheckerFORM.PowerIO11.output_off(SMUon);//open SMUon relay
end;

function
FirstCheckResult(mvoltage,mcurrent:real):integer;
begin
if (mvoltage < 3.3) and (mvoltage > 2.7) and (mcurrent<5*(10e-4)) and (mcurrent> 3*(10e-4)) then
   FirstCheckResult:=1; //all relays correct
if (mvoltage < 3.3) and (mvoltage > 2.7) and (mcurrent>=0) and (mcurrent<=3*(10e-5)) then
   FirstCheckResult:=2; //VCCon relay broken
if (mvoltage <= 0.5) and (mvoltage >= 0) and (mcurrent>=0) and (mcurrent<=3*(10e-5)) then
   FirstCheckResult:=3; //SMUon relay broken
if (mvoltage <= 0.5) and (mvoltage >= 0) and (mcurrent<5*(10e-4)) and (mcurrent> 3*(10e-4)) then
   FirstCheckResult:=4; //ADCon relay broken
end;
else if (mvoltage <= 0.5) and
(mvoltage >= 0) and (mcurrent>=0) and
(mcurrent<=3*(10e-5))then
   FirstCheckResult:=5; // Manual
   check
   //........................situation
   one....................................................//
end;

function
SecondCheckResult(mvoltage2:real):integer;
begin
   if (mvoltage2>4.7) and
   (mvoltage2<5.3) then
      SecondCheckResult:=1 //DACon
   relay correct
   else
      SecondCheckResult:=0; //DACon
   relay broken
end;

procedure
result(VCCimage:integer;DACimage:integer;
ADCimage:integer;SMUimage:integer;SMU2image:integer);
begin
   imageshows(VCCimage);
   imageshows(DACimage);
   imageshows(ADCimage);
   imageshows(SMUimage);
   imageshows(SMU2image);
end;

procedure
Resultshow(FirstResult:integer;SecondResult:Integer;VCCimage1,DACimage1,ADCimage1,SMUimage1,SMU2image1,VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2:
integer);
begin
   if (FirstResult=1) and
   (SecondResult=1) then
      result(VCCimage1,DACimage1,ADCimage1,SMUimage1,SMU2image1)
      else if (FirstResult=1) and
      (SecondResult=2) then
      result(VCCimage1,DACimage2,ADCimage1,SMUimage1,SMU2image1)
      else if (FirstResult=2) and
      (SecondResult=1) then
      result(VCCimage2,DACimage1,ADCimage1,SMUimage1,SMU2image1)
      else if (FirstResult=2) and
      (SecondResult=2) then
      result(VCCimage2,DACimage2,ADCimage1,SMUimage1,SMU2image1)
      else if (FirstResult=3) and
      (SecondResult=1) then
      result(VCCimage1,DACimage1,ADCimage2,SMUimage1,SMU2image1)
      else if (FirstResult=3) and
      (SecondResult=2) then
      result(VCCimage1,DACimage2,ADCimage2,SMUimage1,SMU2image1)
      else if FirstResult=5 then
      result(VCCimage2,DACimage2,ADCimage2,SMUimage2,SMU2image2);
end;
procedure imageno(p:Timage);
begin
  p.Visible:=true;
end;

procedure imagenos(n:Timage);
begin
  n.visible:=false;
end;

procedure imageshows(q:integer);
begin
  case q of
    1: imageno(bdcheckerFORM.image1);
    2: imageno(bdcheckerFORM.image2);
    3: imageno(bdcheckerFORM.image3);
    4: imageno(bdcheckerFORM.image4);
    5: imageno(bdcheckerFORM.image5);
    6: imageno(bdcheckerFORM.image6);
    7: imageno(bdcheckerFORM.image7);
    8: imageno(bdcheckerFORM.image8);
    9: imageno(bdcheckerFORM.image9);
    10: imageno(bdcheckerFORM.image10);
    11: imageno(bdcheckerFORM.image11);
    12: imageno(bdcheckerFORM.image12);
    13: imageno(bdcheckerFORM.image13);
    14: imageno(bdcheckerFORM.image14);
    15: imageno(bdcheckerFORM.image15);
    16: imageno(bdcheckerFORM.image16);
    17: imageno(bdcheckerFORM.image17);
    18: imageno(bdcheckerFORM.image18);
    19: imageno(bdcheckerFORM.image19);
    20: imageno(bdcheckerFORM.image20);
    21: imageno(bdcheckerFORM.image21);
    22: imageno(bdcheckerFORM.image22);
    23: imageno(bdcheckerFORM.image23);
    24: imageno(bdcheckerFORM.image24);
    25: imageno(bdcheckerFORM.image25);
    26: imageno(bdcheckerFORM.image26);
    27: imageno(bdcheckerFORM.image27);
    28: imageno(bdcheckerFORM.image28);
    29: imageno(bdcheckerFORM.image29);
    30: imageno(bdcheckerFORM.image30);
    31: imageno(bdcheckerFORM.image31);
    32: imageno(bdcheckerFORM.image32);
    33: imageno(bdcheckerFORM.image33);
    34: imageno(bdcheckerFORM.image34);
    35: imageno(bdcheckerFORM.image35);
    36: imageno(bdcheckerFORM.image36);
    37: imageno(bdcheckerFORM.image37);
    38: imageno(bdcheckerFORM.image38);
    39: imageno(bdcheckerFORM.image39);
    40: imageno(bdcheckerFORM.image40);
    41: imageno(bdcheckerFORM.image41);
    42: imageno(bdcheckerFORM.image42);
    43: imageno(bdcheckerFORM.image43);
    44: imageno(bdcheckerFORM.image44);
    45: imageno(bdcheckerFORM.image45);
    46: imageno(bdcheckerFORM.image46);
    47: imageno(bdcheckerFORM.image47);
    48: imageno(bdcheckerFORM.image48);
    51: imageno(bdcheckerFORM.image51);
    52: imageno(bdcheckerFORM.image52);
    53: imageno(bdcheckerFORM.image53);
    54: imageno(bdcheckerFORM.image54);
    55: imageno(bdcheckerFORM.image55);
    56: imageno(bdcheckerFORM.image56);
    59: imageno(bdcheckerFORM.image59);
    60: imageno(bdcheckerFORM.image60);
    61: imageno(bdcheckerFORM.image61);
    62: imageno(bdcheckerFORM.image62);
    63: imageno(bdcheckerFORM.image63);
    64: imageno(bdcheckerFORM.image64);
    67: imageno(bdcheckerFORM.image67);
    68: imageno(bdcheckerFORM.image68);
    69: imageno(bdcheckerFORM.image69);
    70: imageno(bdcheckerFORM.image70);
    71: imageno(bdcheckerFORM.image71);
    72: imageno(bdcheckerFORM.image72);
    73: imageno(bdcheckerFORM.image73);
    74: imageno(bdcheckerFORM.image74);
    75: imageno(bdcheckerFORM.image75);
    76: imageno(bdcheckerFORM.image76);
    77: imageno(bdcheckerFORM.image77);
    78: imageno(bdcheckerFORM.image78);
    79: imageno(bdcheckerFORM.image79);
    80: imageno(bdcheckerFORM.image80);
    81: imageno(bdcheckerFORM.image81);
    82: imageno(bdcheckerFORM.image82);
procedure imageNshows(m:integer);
begin
  case m of
    1: imagenos(bdcheckerFORM.image1);
    2: imagenos(bdcheckerFORM.image2);
    3: imagenos(bdcheckerFORM.image3);
    4: imagenos(bdcheckerFORM.image4);
    5: imagenos(bdcheckerFORM.image5);
    6: imagenos(bdcheckerFORM.image6);
    7: imagenos(bdcheckerFORM.image7);
    8: imagenos(bdcheckerFORM.image8);
    9: imagenos(bdcheckerFORM.image9);
   10:imagenos(bdcheckerFORM.image10);
   11:imagenos(bdcheckerFORM.image11);
   12:imagenos(bdcheckerFORM.image12);
   13:imagenos(bdcheckerFORM.image13);
   14:imagenos(bdcheckerFORM.image14);
   15:imagenos(bdcheckerFORM.image15);
   16:imagenos(bdcheckerFORM.image16);
   17:imagenos(bdcheckerFORM.image17);
   18:imagenos(bdcheckerFORM.image18);
   19:imagenos(bdcheckerFORM.image19);
   20:imagenos(bdcheckerFORM.image20);
   21:imagenos(bdcheckerFORM.image21);
   22:imagenos(bdcheckerFORM.image22);
   23:imagenos(bdcheckerFORM.image23);
   24:imagenos(bdcheckerFORM.image24);
   25:imagenos(bdcheckerFORM.image25);
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   27:imagenos(bdcheckerFORM.image27);
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   29:imagenos(bdcheckerFORM.image29);
   30:imagenos(bdcheckerFORM.image30);
   31:imagenos(bdcheckerFORM.image31);
   32:imagenos(bdcheckerFORM.image32);
   33:imagenos(bdcheckerFORM.image33);
   34:imagenos(bdcheckerFORM.image34);
   35:imagenos(bdcheckerFORM.image35);
   36:imagenos(bdcheckerFORM.image36);
   37:imagenos(bdcheckerFORM.image37);
   38:imagenos(bdcheckerFORM.image38);
   39:imagenos(bdcheckerFORM.image39);
   40:imagenos(bdcheckerFORM.image40);
   41:imagenos(bdcheckerFORM.image41);
   42:imagenos(bdcheckerFORM.image42);
   43:imagenos(bdcheckerFORM.image43);
   44:imagenos(bdcheckerFORM.image44);
   45:imagenos(bdcheckerFORM.image45);
   46:imagenos(bdcheckerFORM.image46);
procedure
TbdcheckerFORM.Panel4Click(Sender: TObject);
var
i:integer;
begin
i:=1;
FirstCheckOn(1,19,2,4,5);
FirstComeout(1,19,2,4,5,3,1,1,i+2,i+4,i+6,0,i+1,i+3,i+5,i+7,0);
i:=i+8;
//........pin1............................................./
//
FirstCheckOn(1,19,7,9,10);
FirstComeout(1,19,7,9,10,8,2,2,i+2,i+4,i+6
0, i+1, i+3, i+5, i+7, 0); i:=i+8;
//........pin2............................................../

FirstCheckOn(1, 19, 12, 14, 15, 13, 3, 3, i, i+2, i+4, i+6, 0, i+1, i+3, i+5, i+7, 0); i:=i+8;
//........pin3............................................../

FirstCheckOn(1, 19, 17, 19, 86, 18, 4, 4, i, i+2, i+4, i+6, 0, i+3, i+5, i+7, 0); i:=i+8;
//........pin4............................................../

FirstCheckOn(1, 19, 21, 23, 24, 22, 5, 5, i, i+2, i+4, i+6, 0, i+1, i+3, i+5, i+7, 0); i:=i+8;
//........pin5............................................../

FirstCheckOn(1, 19, 26, 28, 29, 27, 6, 6, i, i+2, i+4, i+6, 0, i+1, i+3, i+5, i+7, 0); i:=i+8;
//........pin6............................................../

FirstCheckOn(1, 19, 31, 33, 0); NoVCCcheck(1, 19, 7, 7, 32, 31, 33, i, i+2, i+4, i+6, 0, i+3, i+5, i+7, 0); i:=i+8;
//........pin7............................................../

FirstCheckOn(1, 19, 35, 37, 0); NoVCCcheck(1, 19, 8, 8, 36, 35, 37, i+2, i+4, i+6, 0, i+3, i+5, i+7, 0); i:=i+8;
//........pin8............................................../

FirstCheckOn(1, 19, 39, 41, 0); NoVCCcheck(1, 19, 9, 9, 40, 39, 41, i+2, i+4, i+6, 0, i+3, i+5, i+7, 0); i:=i+8;
//........pin9............................................../

FirstCheckOn(1, 19, 43, 45, 46, 44, 10, 10, i, i+2, i+4, i+6, 0, i+1, i+3, i+5, i+7, 0); i:=i+8;
//........pin10..........................................//

FirstCheckOn(1, 19, 48, 50, 51, 49, 11, 11, i, i+2, i+4, i+6, 0, i+1, i+3, i+5, i+7, 0); i:=i+8;
//........pin11..........................................//

FirstCheckOn(1, 19, 48, 50, 51, 49, 11, 11, i, i+2, i+4, i+6, 0, i+1, i+3, i+5, i+7, 0); i:=i+8;
//........pin12..........................................//

i:=i+10;
i:=i+8;

//.........pin13..............................................
//
FirstCheckOn(1,19,58,60,0);

NoVCCcheck(1,19,9,9,59,60,58,i+2,i+4,i+6,0
,0,i+3,i+5,i+7,0);
i:=i+8;

//.........pin14..............................................
//

i:=i+8;

//.........pin15..............................................
//
FirstCheckOn(1,19,70,67,0);

NoVCCcheck(1,19,15,15,66,67,70,i+2,i+4,i+
6,0,0,i+3,i+5,i+7,0);

//.........pin16..............................................
//

end;
\textbf{B.2 Index Form}

unit Unit1;

interface

uses
  Windows, Messages, SysUtils, Classes, Graphics, Controls, Forms,
  Dialogs, Menus, jpeg, ExtCtrls, PowerIOdriver, dsi2c, StdCtrls, DAC,
  hardwareform;

type
  TIndex = class(TForm)
  Image1: TImage;
  Image2: TImage;
  DAC1: TDAC;
  MainMenu1: TMainMenu;
  LinTransceiver1: TMenuitem;
  JA10201: TMenuitem;
  JA10211: TMenuitem;
  JA10221: TMenuitem;
  JA10271: TMenuitem;
  JA10281: TMenuitem;
  JA10291: TMenuitem;
  UJA10181: TMenuitem;
  Close1: TMenuItem;
  Calibrate1: TMenuitem;
  BoardChecker1: TMenuitem;
  CurveTracer1: TMenuitem;
  Help1: TMenuitem;
  procedure Close1Click(Sender: TObject);
  private
  \{ Private declarations \}
  \public
  \{ Public declarations \}
end;

\begin{verbatim}
var
  Index: TIndex;

implementation

uses T1020, Unit2, bdchecker;

{$R *.dfm}

procedure TIndex.Close1Click(Sender: TObject);
begin
  close;
end;

procedure TIndex.JA10201Click(Sender: TObject);
begin
  TJA1020.show;
end;

procedure TIndex.FormCreate(Sender: TObject);
var
  IICopen: Boolean;
  dsi2c.speed := 20; \quad \text{// IIC speed on 28kHz}
begin
  IICopen := Init_Controller('EVA A');
  if not IICopen then
    showmessage('no or wrong application board');
  else
    BdCheckerFORM.show;
end;

procedure TIndex.BoardChecker1Click(Sender: TObject);
begin
  BdCheckerFORM.show;
end;
\end{verbatim}

end.
### C. Measurement tools

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<th>Oscilloscope</th>
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